6604 104262

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 09/22/03 Serial # 09/931888 Priority Application Date ______

Your Name Patel, Paresh Examiner # 78089

AU 2829 Phone 306-5859 Room 5B37

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

09-22-03 P03:47 IN

Where have you searched so far on this case?
Circle: (USPT) (DWPI) (EPO Abs) (JPO Abs) (IBM TDB)

Other: Consulted Primaries

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. US 4477774, 6285204
US 3206339, 5006809

What types of references would you like? Please checkmark:

Primary Refs ____ Nonpatent Literature ____ Other ______
Secondary Refs ____ Foreign Patents ____
Teaching Refs ____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

* An insulating film formed on the surface of the electrode (PAD) is broken by probe. The probe is in electrical contact with the electrode or pad.

(Note: breaking of insulation (or oxide) of electrode (or pad) electrically. Not with vibrating the probe or scratching the insulation (or oxide) with probe.

Staff Use Only		Type of Search		Vendors	
Searcher:	JEckhard	Structure (#)		STN	✓
Searcher Phone:		Bibliographic	✓	Dialog	✓
Searcher Location:	STIC-EIC2800, CP4-9C18	Litigation		Questel/Orbit	
Date Searcher Picked Up:	9/29/03	Fulltext		Lexis-Nexis	
Date Completed:	9/29/03	Patent Family		WWW/Internet	
Searcher Prep/Rev Time:	155	Other		Other	
Online Time:	85				

```
SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2003/Sep W3
         (c) 2003 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2003/Sep W4
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
  File   8:Ei Compendex(R)  1970-2003/Sep W3
         (c) 2003 Elsevier Eng.  Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci  1990-2003/Sep W3
         (c) 2003 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2003/Aug
         (c) 2003 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2003/Sep W4
         (c) 2003 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2003/Sep W3
         (c)2003 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Aug
         (c) 2003 The HW Wilson Co.
  File 144:Pascal  1973-2003/Sep W3
         (c) 2003 INIST/CNRS
  File 305:Analytical Abstracts  1980-2003/Sep W1
         (c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2003/Aug
         (c) 2003 DECHEMA
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200361
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/May(Updated 030902)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Apr
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	473517	(INSULAT??????? OR DIELECTRIC??????)(3N)(LAYER??? OR FILM?-?? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER-??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER??)
S2	37375	(BREAK?????? OR BROKE??????? OR DESTROY??????)(3N)(INSULAT-??????? OR DIELECTR??????)
S3	2944469	INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?) OR IC OR -CHIP? ? OR ELECTRODE? ? OR PAD? ?
S4	25077	DIELECTR??????)(3N)(INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?) OR IC OR CHIP? ? OR ELECTRODE? ? OR PAD? ?)
S5	2944469	S3:S4
S6	978	(BREAK?????? OR BROKE????????)(3N)PROBE? ?
S7	798525	PROBE???? OR PROBING
S8	78905	(INSPECT???????? OR ANALYZ??????? OR ANALYS??????)(3N)(PROBE???? OR PROBING OR (INTEGRAT???????)(3N)(CIRCUIT???????? OR LOOP??) OR IC OR CHIP? ? OR ELECTRODE? ? OR PAD? ?)
S9	838489	S7:S8
S10	147	FRIT??????(3N)(PHENOMEN?????? OR APPARAT??????)
S11	469	FRITTING
S12	601	S10:S11
S13	8310	S1 AND S2
S14	3278	S13 AND S5
S15	2	S14 AND S6
S16	2	RD (unique items)
S17	3276	S14 NOT S15
S18	59	S17 AND S9
S19	1	S18 AND S12
S20	58	S18 NOT S19
S21	58	S20 AND S3
S22	13	S21 AND S4
S23	8	RD (unique items)
S24	45	S21 NOT S22
S25	26	S24 AND S7
S26	1	S25 AND S8
S27	25	S25 NOT S26
S28	0	S27 AND S10
S29	0	S27 AND S11
S30	24	RD S27 (unique items)
S31	15	S1 AND S12
S32	15	S31 NOT S21
S33	15	RD (unique items)
S34	6	S2 AND S12
S35	3	S34 NOT S33
S36	2	RD (unique items)
S37	41	S9 AND S12
S38	39	S37 NOT S33,S27,S21
S39	39	S38 AND S9
S40	31	S39 AND S5
S41	0	S40 AND S4
S42	4	S40 AND S8
S43	3	RD (unique items)
S44	27	S40 NOT S42
S45	0	S44 AND S1
S46	27	S44 AND S3
S47	27	S46 AND S7
S48	0	S47 AND S8

16/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02793473
PROBER

PUB. NO.: 01-091073 [JP 1091073 A]
PUBLISHED: April 10, 1989 (19890410)
INVENTOR(s): AMANO NOBUTAKA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-249463 [JP 87249463]
FILED: October 01, 1987 (19871001)
JOURNAL: Section: P, Section No. 902, Vol. 13, No. 322, Pg. 154, July 20, 1989 (19890720)

ABSTRACT

PURPOSE: To achieve a higher ohmic property between a bonding **pad** and a probe for a pellet, by vibrating the probe or a stage carrying a wafer by an ultrasonic wave in a prober used for measuring the wafer of an **integrated circuit**.

CONSTITUTION: A wafer 5 of an **integrated circuit** is carried on a stage 6 to measure. As an ultrasonic wave oscillator 7 is operated when a probe 1 gets in contact with a **pad** aluminum 8 for a pellet, a probe card 3 and the probe 1 vibrate a contact section 30 of the **probe** 1 to **break** any thin **insulation film** 10 on the surface of the **pad** aluminum 8 with the vibration of the probe 1. This can better contact between the **pad** aluminum 8 and the probe 1 thereby allowing a stable inspection of the wafer for the **IC**.

16/3,AB/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

01405647
AXIAL PIN PACKAGE FOR SEMICONDUCTOR **INTEGRATED CIRCUIT**

PUB. NO.: 59-117247 [JP 59117247 A]
PUBLISHED: July 06, 1984 (19840706)
INVENTOR(s): MITANI TSUNEO
KOBAYASHI TORU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-226174 [JP 82226174]
FILED: December 24, 1982 (19821224)
JOURNAL: Section: E, Section No. 275, Vol. 08, No. 235, Pg. 134, October 27, 1984 (19841027)

ABSTRACT

PURPOSE: To improve reliability of tests, by providing a contact **pad**, which is connected to each axial pin, so that sharp needle points **break** an oxidized **insulating film** at the time of the test of an LSI and perfect contact can be obtained.

CONSTITUTION: A **pad** of metal layer is formed in the vicinity of each metal pin 5 on a package base 4 of an axial pin package. When an LSI is tested, probe needles are pushed and contacted to the **pads** 6, and conduction is provided. Even though there is an oxidized **insulating film** and the like, which might be formed on the metal layers, they are **broken** by pushing the **probe** needles 7 to the test **pads** 6 provided on the package, and contact is obtained.

19/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07271079
INSPECTION METHOD AND INSPECTION DEVICE

PUB. NO.: 2002-139542 [JP 2002139542 A]
PUBLISHED: May 17, 2002 (20020517)
INVENTOR(s): IINO SHINJI
TAKEKOSHI KIYOSHI
SUGA TADATOMO
ITO HISAHIRO
KATAOKA KENICHI
APPLICANT(s): TOKYO ELECTRON LTD
SUGA TADATOMO
ITO HISAHIRO
APPL. NO.: 2001-093303 [JP 20011093303]
FILED: March 28, 2001 (20010328)
PRIORITY: 2000-249702 [JP 2000249702], JP (Japan), August 21, 2000 (20000821)

ABSTRACT

PROBLEM TO BE SOLVED: To solve such problems in an inspection method that the service life of a **probe** N is shortened by scrubbing and that yield of a device is reduced by damaging the **inspection electrode** P as shown in (b) of figure 7 when the **probe** N is brought into contact with an **inspection electrode** P electrically by scrubbing operation.

SOLUTION: This inspection method for executing electric characteristic inspection of the device by bringing an **inspection probe** 12A into electric contact with the **inspection electrode** P, has a contact process for bringing the **inspection probe** 12A into electric contact with the **inspection electrode** P by **breaking** an **insulating coat** O of the **inspection electrode** P by utilizing **fritting phenomenon**.

23/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7008457 INSPEC Abstract Number: B2001-09-2130-015
Title: Multifiber ceramic capacitor
Author(s): Chen, L.F.; Hong, Y.P.
Author Affiliation: Dept. of Mater. Sci. & Eng., Xiamen Univ., China
Journal: Journal of Materials Science: Materials in Electronics vol.12, no.3 p.187-91
Publisher: Kluwer Academic Publishers/Chapman & Hall,
Publication Date: March 2001 Country of Publication: USA
CODEN: JSMEEV ISSN: 0957-4522
SICI: 0957-4522(200103)12:3L.187:MCC;1-Y
Material Identity Number: H206-2001-007
U.S. Copyright Clearance Center Code: 0957-4522/2001/$15.00
Language: English
Abstract: A new type of capacitor, multifiber capacitor (MFC) is proposed. It is made up of fiber capacitors (elements) connected in parallel and bonded together with a binder. Each element consists of fiber core (inner **electrode**), **dielectric coating** and outer **electrode**. **Analysis** indicates that MFC has the optimum capacitance in comparison with multilayer capacitor (MLC) when the diameter of fiber core is carefully matched by the thickness of **dielectric coating**. Since **dielectric layer** of a wide range of thickness can be produced more easily as fiber coating than as flat tape, MFC can cover a wider range of capacitance than MLC. Apart from as a possible substitute or supplement to MLC, MFC is potentially useful to bridge the gap between ceramic MLC and thin film capacitor used in **integrated circuits**. MFC also has better resistance to **dielectric breakdown** . The possible techniques for the preparation of MFC are also described.
Subfile: B

23/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5029929 INSPEC Abstract Number: A9518-7860F-002
Title: Surface plasmon-induced luminescence: A **probe** to study electrical aging and **dielectric breakdown** in polymer-like thin films
Author(s): Foulani, A.; Laurent, C.; Canet, P.
Author Affiliation: Lab. de Genie Electr., Univ. Paul Sabatier, Toulouse, France
Journal: Journal of Non-Crystalline Solids Conference Title: J. Non-Cryst. Solids (Netherlands) vol.187 p.415-19
Publication Date: 1 July 1995 Country of Publication: Netherlands
CODEN: JNCSBJ ISSN: 0022-3093
U.S. Copyright Clearance Center Code: 0022-3093/95/$09.50
Conference Title: Amorphous Insulating Thin Films II. E-MRS Spring Meeting, Symposium A
Conference Date: 24-27 May 1994 Conference Location: Strasbourg, France
Language: English

Abstract: Electroluminescence was observed in sandwich structures composed of a thick layer of plasma-deposited hydrogenated carbon and two metallic **electrodes**. Luminescence experiments combined with transport analysis show that the light comes from the radiative decay of **electrode** surface plasmons excited by hot electrons produced in the films. The precise nature of the dielectric is unimportant since the emission process involves the **electrode** parameters. The optical response is governed by the nature and thickness of the positively biased **electrode**: (i) when a thick **electrode** is used, the only excited surface plasmon mode is located at the **dielectric-electrode** interface which acts as a **probe** for the low energy end of the electron energy distribution function; (ii) when a semi-transparent **electrode** is used, electrons with an energy of a few eV can cross the metallic layer. These hot carriers are able to excite a surface plasmon mode located at the outer interface. Depending on the temperature and metal thickness, hot carriers of different kinetic energies can excite this surface plasmon mode. The interface acts as a **probe** for the high energy end of the electron energy distribution function. Detection of luminescence due to **electrode** surface plasmon decay gives access to carrier energy which is the main aging and breakdown controlling factor of the **dielectric layer**.

Subfile: A

23/3,AB/3 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1640265 NTIS Accession Number: AD-A246 834/6

Final Technical Report on Contract N00014-87-K-0494, 1 September 1987 - 31 March 1991 (Minnesota University)

Minnesota Univ., Minneapolis. Dept. of Chemical Engineering and Materials Science.

Corp. Source Codes: 012002164; 406556

24 Feb 92 5p

Languages: English

Journal Announcement: GRAI9212

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A01/MF A01

In research funded by the ONR Young Investigator Award, our group was the first to investigate electrochemical reactions at solid **electrodes** of nanoscopic dimensions. The results have implications in redox chemistry of colloids and supported catalysts and in chemical **analyses** using miniaturized **electrodes**. Initial work using ultra thin platinum band **electrodes** demonstrated a departure of mass-transfer-limited voltammetric currents from predictions based on continuum fluid structure. We proposed an original model that described the dependence of molecular transport on near-surface diffusivity and the dimensions of the reacting electroactive molecule that quantitatively predicts the observed behavior. A detailed theoretical analysis of the effect of the electrical double layer on both electron-transfer kinetics and mass transfer at sub-micron **electrode** structures was developed that indicates that significant departure from the classical voltammetric waveshape and current magnitude is expected when one of the **electrode** dimensions is reduced below 10

nm. A new method of synthesizing Pt disk microelectrodes of nanometer dimensions was developed based on using a scanning tunneling microscope (STM) to induce localized **dielectric breakdown** on TiO2 **coated** Pt substrates.

23/3,AB/4 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

0513173 NTIS Accession Number: AD-A013 935/2/XAB
Study of Electronic Transport and **Breakdown** in Thin **Insulating Films**
(Semi-annual technical rept. no. 5)
Johnson, W. C. ; Bottoms, W. R.
Princeton Univ N J Dept of Electrical Engineering
Corp. Source Codes: 400734
Sponsor: Air Force Cambridge Research Labs., Hanscom AFB, Mass.; Defense Advanced Research Projects Agency, Arlington, Va.
Report No.: AFCRL-TR-75-0157
Jan 75 20p
Journal Announcement: GRAI7521
See also report dated Jan 74, AD-783 870.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
An overview is given of progress in the study of high-field electronic transport and **dielectric breakdown** in thin (1000-5000 A) **insulating films** on silicon. The principal results to date are on SiO2; also under study are Al2O3, Si3N4, and layered composites. The studies include corona-induced nondestructive breakdown, self-quenched breakdown, effects of electron irradiation, study of charge-carrier trapping, study of lateral nonuniformities, electron-beam **probing** of the insulator-semiconductor interface, and theoretical modeling of hot-electron distributions and of localized breakdown.

23/3,AB/5 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

0440430 NTIS Accession Number: AD-777 915/0/XAB
Study of Electronic Transport and **Breakdown** in Thin **Insulating Films**
(Semi-Annual technical rept. no. 1)
Lampert, M. A. ; Johnson, W. C. ; Bottoms, W. R.
Princeton Univ N J Dept of Electrical Engineering
Corp. Source Codes: 400734
Report No.: AFCRL-TR-73-0263
Jan 73 98p
Journal Announcement: GRAI7413
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A05/MF A01

A comprehensive research program is under way for the characterization of electronic transport and **dielectric** breakdown properties of thin **insulating films** on Si which are technologically important, namely SiO2, Al2O3, Si3N4 and their composites. The main experimental approaches are: Non-destructive breakdown of un-metallized films exposed to a corona discharge in a suitable gas (dry air, N2, rare gas, etc.), locally destructive, self-quenching breakdown of MIS capacitor structures, optical charge - optical and thermal discharge studies of electronic traps in the films, kilovolt electron-beam **probe** studies of the films, including damage induced by the beam. Accompanying theoretical studies initially are concerned with Monte Carlo calculations of hot-electron distributions induced by high electric fields in the film. (Modified author abstract)

23/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05504733
E.I. No: EIP00035087881
Title: Fabrication of counter **electrodes** for scanning atomic **probe**
Author: Campitelli, A.; Ziad, H.; Rogge, F.; Vandervorst, W.; Baert, K.; Huang, M.; Cerezo, A.
Corporate Source: IMEC, Leuven, Belgium
Conference Title: Proceedings of the 1999 Micromachining and Microfabrication Process Technology V
Conference Location: Santa Clara, CA, USA Conference Date: 19990920-19990922
E.I. Conference No.: 56136
Source: Proceedings of SPIE - The International Society for Optical Engineering v 3874 1999. p 138-149
Publication Year: 1999
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: This paper reports on the fabrication of innovative counter **electrodes** for the development of a new Scanning Atom **Probe** (SAP) instrument. A process using thick spin-on dielectrics (BenzoCycloButene), deep reactive ion etching (DRIE) and photolithography (both standard and electroplated) has been developed for the realisation of the counter **electrodes**. The novel structure is a two-terminal device in the form of a hollow cone shape, with two **electrodes** separated by a **dielectric layer** (high **breakdown** voltage **insulator**). Different counter **electrode** design versions are presented, with the focus on the results for the first iteration. Electrical testing of the **insulating layer** is performed to investigate the material suitability for the operating conditions of the SAP instrument. Details regarding the design and fabrication procedure for the different designs, with emphasis on the process flow for the non standard steps, are also presented. (Author abstract) 4 Refs.

23/3,AB/7 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05392887
E.I. No: E2099104835186

Title: Study of Ta//2O//5/rugged Si capacitor of 23 μ C/ μ m**2 applied to high-density DRAMs using sub-0.2 μ m process
Author: Ohji, Y.; Iijima, S.; Saito, A.; Miki, H.; Kanai, M.; Kunitomo, M.; Yamamoto, S.; Furukawa, R.; Sugawara, Y.; Uemura, T.; Kuroda, J.; Nakata, M.; Kisu, T.; Kawagoe, T.; Kawakita, K.; et al
Corporate Source: Hitachi Ltd, Tokyo, Jpn
Conference Title: Proceedings of the 1999 37th Annual IEEE International Reliability Physics Symposium
Conference Location: San Diego, CA, USA Conference Date: 19990323-19990325
E.I. Conference No.: 55372
Source: Annual Proceedings - Reliability Physics (Symposium) 1999. p 12-18
Publication Year: 1999
CODEN: ARLPBI ISSN: 0099-9512 ISBN: 0-7803-5220-3
Language: English
Abstract: The Ta//2O//5/rugged-Si capacitor was shown to be remarkably reliable for mass production of high-density DRAMs. Our investigation with large scale test capacitors and full-scale 64-Mbit and 256-Mbit DRAMs confirmed that it has low leakage current, low defect density, good retention characteristics, and superior TDDB lifetime for the high-density DRAMs. (Author abstract) 14 Refs.

23/3,AB/8 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02750438
ACTIVE MATRIX ARRAY

PUB. NO.: 01-048038 [JP 1048038 A]
PUBLISHED: February 22, 1989 (19890222)
INVENTOR(s): TAKAHARA HIROSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-204651 [JP 87204651]
FILED: August 18, 1987 (19870818)
JOURNAL: Section: P, Section No. 881, Vol. 13, No. 245, Pg. 138, June 08, 1989 (19890608)

ABSTRACT

PURPOSE: To correct the defect of an active matrix array by disconnecting a defective thin film transistor TFT from picture element **electrodes** and impressing a voltage between a conductive connecting wiring and the picture element **electrode**, thereby inducing **dielectric breakdown** between the **insulating** wiring and the picture element **electrode** and electrically connecting the picture element **electrode** and the adjacent picture element **electrode** via the connecting wiring.

CONSTITUTION: The active matrix array is used for a liquid crystal panel and a 1st **insulator film** 12 is formed on gate and source signal wires 3, 4 formed between the 1st and 2nd picture element **electrodes** 1a and 1c. A 2nd **insulator film** 13 consisting of an inorganic material is formed between the **electrode** 1c and the conductive connecting wiring 14 to maintain electrical insulation. A drain terminal 5 of the defective TFT is disconnected from the **electrode** 1a and a

probe 16 is brought into pressurized contact with the surface of the **electrode** 1a or the connecting wiring 14 and a **probe** 17 with the **electrode** 1c. The prescribed voltage from a voltage impressing means 18 is impressed to the **electrodes** via a switch 19 to **break** down the **insulation** of the **insulator film** 13 by which the connecting wiring 14 and the **electrode** 1c are electrically connected.

26/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03765648
MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 04-130748 [JP 4130748 A]
PUBLISHED: May 01, 1992 (19920501)
INVENTOR(s): TEZUKA IZUMI
INABA TORU
NAGANUMA YOSHIMI
INOUE MASAHIRO
UCHIDA HIROMI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI TOBU SEMICONDUCTOR LTD [470867] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-252286 [JP 90252286]
FILED: September 21, 1990 (19900921)
JOURNAL: Section: E, Section No. 1252, Vol. 16, No. 397, Pg. 80, August 24, 1992 (19920824)

ABSTRACT

PURPOSE: To screen all MIS capacities with high accuracy and surely by a method wherein an **electrode** for capacity **inspection** use is formed at the stage of a wafer, a definite voltage is applied, a MIS capacity having a possibility of a failure at an early stage is destroyed and the **electrode** for capacity **inspection** use is removed.

CONSTITUTION: An **insulating film** 8 by an SiO(sub 2) film is formed selectively on the main face of a wafer 20; and **electrodes** 32, 33, for capacity inspection use, which are composed of Al are formed at contact holes 30, 31 where the **insulating film** 8 has not been formed. The **electrodes** 32 for capacity **inspection** use on one side are overlapped with an **insulating film** 4 for capacity use so as to come into contact with it; and the **electrodes** 33 for capacity **inspection** use on the other side are overlapped with a capacity formation part 2 so as to come into contact with the part. **Probe** needles 40 for a wafer **prober** are pushed to **inspection** terminals 36 in a **chip** region 34, and an inspection voltage is applied. An intrinsic **dielectric breakdown** voltage of an Si(sub 3)N(sub 4) film is applied to the **insulating film** 4 for capacity use for a short time of less than one second; and a capacity is destroyed so as to cause a failure at an early stage. Then, the **insulating film** 4, for capacity use, which has been destroyed by the wafer **prober** is detected; then, the **electrodes** 32, 33 for capacity inspection use are etched and removed.

30/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7530349 INSPEC Abstract Number: A2003-06-8160C-018, B2003-03-2550E-053
Title: Bias-induced spatially resolved growth and removal of Si-oxide by atomic force microscopy
Author(s): Myhra, S.
Author Affiliation: Sch. of Sci., Griffith Univ., Nathan, Qld., Australia
Journal: Applied Physics A (Materials Science Processing) vol.A76, no.1 p.63-9
Publisher: Springer-Verlag,
Publication Date: Jan. 2003 Country of Publication: Germany
CODEN: APAMFC ISSN: 0947-8396
SICI: 0947-8396(200301)A76:1L.63:BISR;1-3
Material Identity Number: D218-2002-014
Language: English
Abstract: Three mechanisms for spatially resolved growth and removal of oxide on silicon substrates have been investigated. Thermally grown oxide layers with thicknesses in the range 2-6 nm were the distinctive feature of the system. The layers were characterized and manipulated by methodologies based on atomic force microscopy (AFM) with conducting **probes** in a vacuum environment of 10/sup -2/-10/sup -3/ Pa. The **probe** is then effectively a travelling **electrode** that generates an electrostatic field between the tip and the substrate. Oxide growth was induced for a positive sample bias greater than 5 V, but below the level corresponding to **dielectric breakdown**. Application of a short pulse of amplitude marginally above that corresponding to **dielectric breakdown**, on the other hand, had the effect of producing pits of inner diameter of about 10 nm in the pre-existing oxide layer at the point of tip-to-oxide contact. Application of a low positive sample bias (less than that required for measurable oxide growth) in combination with high linear scan speed had the effect of removing a pre-existing oxide layer from the scanned field of view. The most plausible mechanisms are based on transverse ionic diffusion (for oxide growth), controlled **dielectric breakdown** (for formation of pits) and lateral transport of silicaceous species (for oxide removal).
Subfile: A B

30/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7045487 INSPEC Abstract Number: B2001-11-2570D-004
Title: Reliability monitoring and screening issues with ultrathin gate dielectric devices
Author(s): Abadeer, W.W.
Author Affiliation: Microelectron. Div., IBM Corp., Essex Junction, VT, USA
Journal: IEEE Transactions on Device and Materials Reliability vol.1, no.1 p.60-8
Publisher: IEEE,
Publication Date: March 2001 Country of Publication: USA
CODEN: ITDMA2 ISSN: 1530-4388
SICI: 1530-4388(200103)1:1L.60:RMSI;1-U

Material Identity Number: H574-2001-001
U.S. Copyright Clearance Center Code: 1530-4388/2001/$10.00
Language: English
Abstract: Installing appropriate quality and reliability monitoring procedures for ultrathin gate dielectrics is of utmost importance. Ensuring the integrity of VLSI products and unwavering customer satisfaction are the top priorities. Several key strategic avenues have been pursued to accomplish those priorities. First, basic tool and processing monitoring and measurement procedures are put into place for categories such as metallic contamination, foreign material control, and semiconductor stress-induced defects such as dislocations and stacking faults. Second, a new voltage ramp breakdown test, especially designed for ultrathin gate dielectrics, is installed based on a one-to-one correlation with TDDB testing, from which a fail criterion for minimum required breakdown voltage of the distribution is defined. The voltage ramp test is capable of identifying weaknesses or failures for either the intrinsic or extrinsic parts of the failure rate distribution. The voltage ramp test is installed at various processing levels starting with post silicide **probing** (PSP) utilizing very large guide area/perimeter structures (area>0.5 mm/sup 2//**chip**, and perimeter >1 meter/**chip**) with both shallow trench isolation (STI) and diffusion perimeters. Third, a voltage breakdown test is put into place for in-line charging effects at various processing levels. The structure used employs minimum polysilicon linewidth devices and contains a nonantenna reference device as well as a variety of antenna structures for various design levels starting with polysilicon and including all via, contact, and metal levels. Such a **dielectric breakdown** test for charging is also well correlated with other device failure mechanisms such as hot carriers. Fourth, a new methodology was adopted based on a one-to-one quantitative correlation between lifetime as derived from accelerated TDDB testing and the initial value of gate dielectric leakage at a predetermined value(s) of voltage(s). This excellent correlation was verified for gate dielectric thickness ranging from 10 nm to below 3 nm. Fifth, at product level, the standby I/sub ddQ/ and I/sub dd/ currents are measured and tracked for changes under accelerated stress conditions for numerous scan chains. This measurement is a good indicator of the defect level on products and the overall impact of ultrathin gate dielectric on product yield and reliability. Finally, various types of voltage screens and burn-in with duration ranging from few seconds to several hours (at wafer and packaged levels) can be implemented (at least on a selected set of products) to monitor and/ improve the reliability of the final assembly. Accordingly, the body of the text discusses the following topics: monitoring of gate dielectric reliability, monitoring of device stability, monitoring of thin dielectric initial leakage, semiconductor stress induced defects, metallic contamination, and reliability of **integrated circuits**.
Subfile: B

30/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5958718 INSPEC Abstract Number: B9808-2570F-003
Title: Monitoring of dielectric quality with mercury (Hg) gate MOS current-voltage (Hg-MOSIV)
Author(s): Hillard, R.J.; Mazur, R.G.; Gruber, G.A.; Sherbondy, J.C.
Author Affiliation: Solid State Measure. Inc., Pittsburgh, PA, USA

Conference Title: Proceedings of Electrochemical Society Symposium on Diagnostic Techniques for Semiconductor Materials and Devices (ECS PV 97-12; SPIE vol.3322) p.310-23
Editor(s): Rai-Choudhury, P.; Benton, J.L.; Schroder, D.K.; Shaffner, T.J.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA ix+478 pp.
Material Identity Number: XX96-03646
Conference Title: Diagnostic Techniques for Semiconductor Materials and Devices
Conference Sponsor: Electrochem. Soc
Conference Date: 6-8 May 1997 Conference Location: Montreal, Que., Canada
Language: English
Abstract: MOS gate dielectric quality is strongly dependent on process induced defects, substrate quality, dielectric formation and stoichiometry. In the past, these defects have been monitored with MOS capacitors (MOSCAPs) with polysilicon or deposited metal gates. The additional processing required to form these gates is time consuming and may introduce additional defects. An alternate gate that is sensitive and can provide immediate feedback is highly desirable. This paper demonstrates the use of a high repeatability Hg **probe** for the monitoring of dielectric quality with MOS IV based time zero **dielectric breakdown** (TZDB) and TDDB methods. Three major issues are discussed in detail; these are the physics of Hg gate MOS IV measurements and their repeatability and sensitivity to defects.
Subfile: B

30/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

01455315 INSPEC Abstract Number: A80015975, B80004790
Title: High field conduction and **breakdown** in corona charged **insulating films**
Author(s): Coelho, R.
Author Affiliation: Lab. de Phys. des Decharges, Ecole Superieure d'Electricite, CNRS, Gif sur Yvette, France
Conference Title: Third International Conference on Dielectric Materials, Measurements and Applications p.200-2
Publisher: IEE, London, UK
Publication Date: 1979 Country of Publication: UK xii+418 pp.
Conference Sponsor: IEE
Conference Date: 10-13 Sept. 1979 Conference Location: Birmingham, UK
Language: English
Abstract: The author attempts to show that the ionized air of a DC corona discharge can be used as a convenient **electrode** for quick and easy estimations of the conduction current and the **breakdown** field in thin **insulating films**. While the corona is on, the potential on the exposed surface differs from the tip voltage by an amount which may exceed 5 kV and is not easy to measure. This problem is discussed and it is shown that proper use of an electrostatic **probe**, and of the characteristics of the corona, may help a great deal toward its solution.
Subfile: A B

30/3,AB/5 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

0570457 NTIS Accession Number: AD-A028 884/5/XAB
The Physics of Reliability of Future Electronic Devices
(Final rept. 1 Jun 74-30 Nov 76)
DiStefano, T. H. ; Tu, K. N.
IBM Thomas J Watson Research Center Yorktown Heights N Y
Corp. Source Codes: 349250
Report No.: RADC-TR-76-160
May 76 110p
Journal Announcement: GRAI7622
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A06/MF A01
Among the major reliability problems in semiconductor devices are semiconductor surface defects, **dielectric breakdown** , interdiffusion across interfaces, and corrosion. In the area of surface defects, the authors have used scanned optical techniques to **probe** defects and recombination centers on silicon surfaces. Crystallographic defects on silicon surfaces, of the type measured by the scanned optical techniques are known to promote device failure. The problem of **dielectric breakdown** in SiO2, which is particularly important to the reliability of **integrated circuits**, was investigated both theoretically and experimentally. Interface reactions were found to be particularly important to the reliability of Schottky barriers. Several classifications of metals have been determined and studied with respect to their behavior in the formation of metal silicide Schottky barrier contacts to silicon. On the basis of the classification of reaction properties, the reaction between the metal and either silicon or SiO2 can be explained and understood.

30/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04022017
E.I. No: EIP94122498997
Title: Electroluminescence from radiative decay of surface plasmons in aluminum-insulator-indium tin oxide structures
Author: Canet, P.; Laurent, C.
Corporate Source: Universite Aix-Marseille, Fr
Source: Journal of Applied Physics v 75 n 11 June 1994. p 7460-7464
Publication Year: 1994
CODEN: JAPIAU ISSN: 0021-8979
Language: English
Abstract: Further evidence for an emission process implicating surface plasmon (SP) decay was presented. The positively biased **electrode** was deposited on glass and comprised of a thick indium-tin-oxide layer or a thin aluminum film. In both cases, the **dielectric** was a **layer** of amorphous hydrogenated carbon (a-C:H) formed by glow discharge polymerization. Excitation conditions and coupling between SP and photons were also discussed. It was shown that determining the relative contribution of SP modes to the final radiative output of the

metal-insulator-metal structure by analyzing the temperature dependence of the emission efficiency and of the light spectra was achievable. The external surface of the metallic **electrode** served as a **probe** for electrons with higher energies. This can be very advantageous in understanding **dielectric breakdown** and electrical aging of the **insulating layer**. 15 Refs.

30/3,AB/7 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03888824 Genuine Article#: QN571 Number of References: 11
Title: HETEROEPITAXIAL GROWTH OF SRVO3-X AND SRTIO3 FILMS ON SI SUBSTRATES AND FORMATION OF LAYERED STRUCTURES (Abstract Available)
Author(s): MOON BK; ISHIWARA H
Corporate Source: TOKYO INST TECHNOL,PRECIS & INTELLIGENCE LAB,MIDORI KU/YOKOHAMA/KANAGAWA 227/JAPAN/
Journal: JOURNAL OF THE KOREAN PHYSICAL SOCIETY, 1995, V28, S (FEB), P S60-S64
ISSN: 0374-4884
Language: ENGLISH Document Type: ARTICLE
Abstract: Heteroepitaxial growth of conductive SrVO3-x, (SVO) and high-**dielectric** SrTiO3 **films** on Si(100) substrates is conducted using a focused electron beam evaporation method. In order to realize direct growth of these films on Si substrates, we propose a Sr-deoxidation method in this study. It has been found from the results of X-ray diffraction analyses and pole figure measurement that the epitaxial relationships between SVO or STO and Si(100) substrate are (100)(SVO)//(100)Si, <001>(SVO)//<001>(Si) and (100)(STO)//(100)Si, <001>(STO)//<001>(Si). It has also been observed from the depth-profiling by Auger electron spectroscopy that an STO film has a stoichiometric composition and interdiffusion hardly that an STO film has a stoichiometric composition and interdiffusion hardly occurs at the interface. From the result of a dc four-point **probe** measurement, the lowest electrical resistivity obtained at RT was 346 mu Omega cm in case of an SVO film. Applications of SVO and STO films are so proposed as to use them as a crystalline **electrode** and a diffusion bearrier, respectively. In the case of STO/SVO/Si structure, excellent electrical properties of STO films were obtained, in which the best values of **breakdown** field, resistivity and **dielectric** constant were 345 kV/cm, 6.4x10(12) Omega cm and 243, respectively. Finally, it is attempted to form a PbZrxTi1-xO3 (PZT) film on the STO/Si(100) substrate using sol-gel method.

30/3,AB/8 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01124760 Genuine Article#: FY343 Number of References: 33
Title: SURFACE CHARGING AND FLASHOVER OF SPACERS IN SF6 UNDER IMPULSE VOLTAGES (Abstract Available)
Author(s): SRIVASTAVA KD; ZHOU JP
Corporate Source: UNIV BRITISH COLUMBIA,DEPT ELECT ENGN/VANCOUVERV6T 1W5/BC/CANADA/
Journal: IEEE TRANSACTIONS ON ELECTRICAL INSULATION, 1991, V26, N3, P 428-442

Language: ENGLISH Document Type: ARTICLE
Abstract: In compressed gas insulated transmission line and sub-station equipment support spacers may determine the overall insulation integrity. Surface charges have been observed on spacers under normal operation and before equipment flashover. The paper describes a series of experiments to study prebreakdown spacer charging, and subsequent flashover, in a compressed gas **insulated** rod-**spacer**-plane system under positive impulse voltages. Pre-breakdown corona is identified as the most likely source for spacer charging. Surface charges were measured in situ with capacitive **probes** after the applied lightning impulse voltage had decayed to zero. Numerical computation of resultant electric fields, using the surface charge simulation method, shows that the electric field due to surface charges significantly lowers the electric field near the rod **electrode** but enhances the overall electric field over the rest of the spacer surface. The flashover voltage with a spacer is higher than for a rod-plane gap. A reversal of the applied impulse polarity may, however, drastically lower the flashover voltage for a rod-spacer-plane gap.

30/3,AB/9 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04004066 JICST ACCESSION NUMBER: 99A0264058 FILE SEGMENT: JICST-E
Silicon dioxide with low dielectric constant using liquid phase deposition method.
CHANTHAMALY P (1); ARAKAWA TARO (1); HANEJI NOBUO (1)
(1) Yokohama Natl. Univ., Fac. of Eng.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1999, VOL.98,NO.555(SDM98 184-191), PAGE.51-57, FIG.9, TBL.2, REF.18
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 539.23:546
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This work we present a method that can grow SiO2:F film in supersaturated fluorsilicic acid(H2SiF6) at 35.DEG.C.. XPS measurement results an insertion of F atome are during 3.5% to 4.75% in this **film**. It's **dielectric** constant were of observed to have values of 3.7 to 3.0 as a function of H2SiF6 concentration from 2.00mol/l to 3.25mol/l respectively. The I-V results showed a sufficiently high **dielectrical breakdown** field of more than 9MV/cm. It's electrical strength indicate the utility of this method on the field of **multilayer dielectric films** and/or planarization application, and exept that AFM images show very low bumpy surface shape less than 0.5nm. (author abst.)

30/3,AB/10 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03566604 JICST ACCESSION NUMBER: 98A0479617 FILE SEGMENT: JICST-E
Advanced Memory Devices Using High-.EPSILON. and Ferroelectric Films.

Limitations on ULSI-FeRAMs.
SCOTT J F (1)
(1) Max Planck Inst. Microstructal Physics Halle, Saale, DEU
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1998, VOL.E81-C,NO.4, PAGE.477-487, FIG.11, REF.54
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 537.226.4
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A review of fundamental and practical limitations on ferroelectric thin-film non-volatile random access memories is given. Size effects are considered (both thickness and lateral dimensions) from the point of view of both depolarization field instabilities and electrical breakdown mechanisms. Emphasis is on switched-capacitor pass-gate architectures, but true ferroelectric FETs (in which the metal gate in the field-effect transistor is replaced with a ferroelectric film) are discussed briefly. The conclusion is that ferroelectric non-volatile RAMs of Gigabit densities are technically viable in the immediate future. (author abst.)

30/3,AB/11 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02979986 JICST ACCESSION NUMBER: 96A0720960 FILE SEGMENT: JICST-E
Reduction of Electron Shading Damage Using Synchronous Bias in Pulsed Plasma.
HASHIMOTO K (1); HIKOSAKA Y (1); HASEGAWA A (1); NAKAMURA M (1)
(1) Fujitsu Ltd., Kawasaki, JPN
Jpn J Appl Phys Part 1, 1996, VOL.35,NO.6A, PAGE.3363-3368, FIG.19, REF.10
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 533.9.06 621.382.002.2
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A novel method is proposed for reducing charging damage due to the "electron shading" effect. The concept is to selectively utilize the coolest electrons in a pulsed plasma at the end of its off period by synchronizing rf bias; thereby one should be able to reduce the negative charge build-up responsible for the damage. This concept has been examined using an inductively coupled plasma (ICP) apparatus. Exposure to a cw Ar ICP damaged most MOS capacitors with a 6-nm-thick gate oxide and connected to 105 shaded antennas. This damage was reduced only slightly even with 5-.MU.s-on/10-.MU.s-off pulse modulation when the rf bias was asynchronous (60 kHz). When the rf bias (66.7 kHz) synchronized at the expected optimal phase, the most significant reduction of the damage was observed. This effect is discussed based on the results of time-resolved **probe** and optical emission m easurements. (author abst.)

30/3,AB/12 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02192042 JICST ACCESSION NUMBER: 94A0593949 FILE SEGMENT: JICST-E
Special issue : On a high reliability gate oxide film. Present situation and problems of the furnace related apparatus and the material technology.
HASEGAWA EIJI (1)
(1) NEC Corp.
Gekkan Semiconductor World(Semiconductor World), 1994, VOL.13,NO.7, PAGE.104-108, FIG.6, REF.11
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: In the present situation where the gate oxide film gets thinner and the thickness of 4-5nm is used, the control of a natural oxidation film and an interface becomes a problem. This paper describes problems and measures of the ultrathin **insulating film** forming technology and equipment, including a nitriding oxide film which is considered important lately. This paper describes the ultrathin oxide film forming technology, the in-furnace atmosphere dependence of the reliability of the gate oxide film, the nitriding oxide film forming technology, the LPCVD equipment, etc. in detail.

30/3,AB/13 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01038174 JICST ACCESSION NUMBER: 90A0328195 FILE SEGMENT: JICST-E
Special edition : maintenance and simple diagnostic tool. Live-line diagnosis using an insulation monitor.
TOKUDA TAKASHI (1)
(1) Meidensha Corp.
Denki to Kanri, 1990, VOL.31,NO.4, PAGE.31-37, FIG.12, TBL.3, REF.9
JOURNAL NUMBER: S0256ABE ISSN NO: 0388-4031
UNIVERSAL DECIMAL CLASSIFICATION: 621.313.1
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes the present situation of live-line diagnosis of a high voltage rotating machine on a following item.1) insulation degradation (degradation factors degradation phenomenon and deterioration mechanisms);2) degradation diagnostic methods ;3) the live-line insulation diagnosis method (a method for installing a sensor in coil low-resistant ply, a method for installing an **electrode** in a slot, and a method by magnetic **probe**, a method by a coupling capacitor, a method for equipping semiconductor **layer** into **insulating** one, a method by vibrational analysis and a method by grain detection ;4) problems.

30/3,AB/14 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015087140
WPI Acc No: 2003-147658/200314
Related WPI Acc No: 2002-673037
XRAM Acc No: C03-038070
XRPX Acc No: N03-116610
Bonding **pad** has partially completed silicon **integrated circuit**, first hollow square trench, barrier layer, metal **layer**, cap **layer**, second **dielectric layer**, **broken** line hollow square via hole, and aluminum bonding **pad**
Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)
Inventor: CHU T Y; HSIA C C; TSUI B; YANG T
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020149115	A1	20021017	US 2000713801	A	20001116	200314 B
			US 2002170124	A	20020612	
US 6566752	B2	20030520	US 2000713801	A	20001116	200336
			US 2002170124	A	20020612	

Priority Applications (No Type Date): US 2000713801 A 20001116; US 2002170124 A 20020612
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020149115	A1		7	H01L-023/48	Div ex application US 2000713801
					Div ex patent US 6426555
US 6566752	B2			H01L-029/40	Div ex application US 2000713801
					Div ex patent US 6426555

Abstract (Basic): US 20020149115 A1
Abstract (Basic):
NOVELTY - A bonding **pad** comprises:
(i) a partially completed silicon **integrated circuit**;
(ii) a first trench in the shape of a hollow square;
(iii) a barrier layer;
(iv) a metal layer;
(v) a cap layer;
(vi) a second **dielectric layer**;
(vii) a via hole in the shape of a broken line hollow square that is disposed to lie entirely within the first hollow square; and
(viii) an aluminum bonding **pad** that fills and fully overlaps the via hole.
DETAILED DESCRIPTION - A bonding **pad** comprises a partially completed silicon **integrated circuit** that includes an uppermost **layer** of a first **dielectric** material having a first upper surface; a first trench, having a first width, in the shape of a hollow square (54) that extends downwards from the first surface to a depth; a barrier layer (41) over the upper surface and including the first trench; a metal layer that fills the first trench; a cap layer (42) over the upper surface and the metal **layer**; a second **dielectric layer** over the cap layer and having a second upper surface; a via hole (32), having a second width less than the first width, in the shape of a broken line hollow square that is disposed to lie entirely within the first hollow square and that extends below the second upper surface, through the second **dielectric layer** and the cap layer, to the metal layer; and an aluminum bonding **pad** on the second upper surface that fills and fully overlaps the via hole.
An INDEPENDENT CLAIM is included for a process of manufacturing the

bonding **pad**, comprising providing the partially completed silicon **integrated circuit** having as its uppermost **layer** a first **dielectric layer** (15) having a first upper surface; forming the first trench in the shape of the hollow square that extends downwards from the first upper surface to the depth; depositing the barrier layer over the upper surface and the trench; overfilling the trench with metal and then planarizing, thus forming a damascene structure where the trench is just filled with metal; depositing a cap layer over the upper surface, including all exposed metal, followed by the second **dielectric layer**; forming the via hole in the shape of the broken line hollow square that is disposed to lie entirely within the first hollow square and that extends downwards from the second upper surface, through the second **dielectric layer** and the cap layer, to expose the metal layer; and depositing an aluminum layer (33) on the second upper surface and then patterning and etching the aluminum to form the bonding **pad**. The **pad** fills and fully overlaps the via hole.

USE - As a bonding **pad**.

ADVANTAGE - The inventive bonding **pad** has a low parasitic capacitance, and transmits little or no stress to the underlying metal layer during bonding. It protects a damascene conductor from damage during electrical **probing** and wire bonding.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a bonding **pad**.

First **dielectric layer** (15)
Via hole (32)
Aluminum layer (33)
Barrier layer (41)
Cap layer (42)
Silicon oxide layer (43)
Silicon nitride layer (44)
Hollow square (54)
pp; 7 DwgNo 5/12

30/3,AB/15 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010972313
WPI Acc No: 1996-469262/199647
XRPX Acc No: N96-395501
Information recording and reproducing appts. using scanning type **probe** - has piezo element controller which controls piezo element for **probe electrode** drive to maintain constant distance between **probe electrode** and recording medium
Patent Assignee: SHARP KK (SHAF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8235653	A	19960913	JP 9538703	A	19950227	199647	B

Priority Applications (No Type Date): JP 9538703 A 19950227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8235653	A		3	G11B-009/04	

Abstract (Basic): JP 8235653 A

The appts. has a **probe electrode** (2) which detects a scanned area of a recording medium (1) surface and the electrical resistance value changed by **dielectric breakdowns** before reading an information. A current measuring device (4) measures the current value associated with the scanning of the **probe electrode**.

A controller (6) controls the piezo element (5) used for a **probe electrode** drive maintaining a constant distance or gap between the **probe** and the recording medium intermediation surface. An information is written in w.r.t. recording medium surface using the **dielectric** breakdown of an **insulated** thin **film**.

ADVANTAGE - Stabilises information writing in process.

Dwg.1/2

30/3,AB/16 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

001832017
WPI Acc No: 1977-53014Y/197730
Contact **electrode** in semiconductor - by depositing **insulating film** under silane atmos., selectively irradiating with laser to break film and decompose silane to form **electrode**
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 52070762	A	19770613				197730	B

Priority Applications (No Type Date): JP 75146650 A 19751209

Abstract (Basic): JP 52070762 A

Semiconductor device is provided with metal wiring means impurity diffused region or polycrystalline silicon and an **insulating layer** of silicon dioxide are deposited in an atmos. of silane (SiH4) gas diluted with nitrogen gas. Laser beam having beam dia. of several microns is irradiated onto the predetermined portion of the wiring to form an **electrode**. The irradiated portion is heated by the laser beam energy to **break** the **insulating film** and at the same time SiH4 is thermally decomposed to form a polycrystalline **electrode** into which impurities in the wiring are doped.

A small size **electrode** is obtd. to which a measuring **probe** is easily connected. The method is preferably used for measuring and repairing the break down of wiring in an **integrated circuit**.

30/3,AB/17 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03769742
METHOD AND DEVICE FOR EVALUATING RELIABILITY OF **INSULATING FILM**

PUB. NO.: 04-134842 [JP 4134842 A]

PUBLISHED: May 08, 1992 (19920508)
INVENTOR(s): OZAWA YOSHIO
YAMABE KIKUO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-255114 [JP 90255114]
FILED: September 27, 1990 (19900927)
JOURNAL: Section: E, Section No. 1254, Vol. 16, No. 403, Pg. 99, August 26, 1992 (19920826)

ABSTRACT

PURPOSE: To enable complete selection and removal of a semiconductor device which causes initial troubles without lowering final yield and life by carrying out heat treatment after applying a high electric field between an **electrode** and a semiconductor wafer and by applying an electric field thereafter.

CONSTITUTION: A specified high electric field is applied for a specified time between an **electrode** 4 and a silicon substrate 1 with a **probing** needle in contact with an upper **electrode** 4 of each division, and electron is made to flow in a direction from the **electrode** 4 to the substrate 1. Thereby, a gate **insulating film** having defects permanently breakdowns and charge is trapped in a gate **insulating film** without defects. Thereafter, heat treatment is performed for the silicon substrate in an inert atmosphere, and the charge trapped in the gate **insulating film** is reduced. After manufacture of a semiconductor **integrated circuit** is completed by a usual method, a voltage is applied between the **electrode** 4 and a diffusion layer 3 and a usual screening test is performed. Thereby, it is possible to remove a semiconductor device which causes **dielectric breakdown** caused by defects without lowering the intrinsic **dielectric breakdown** life of a gate **insulating film** without defects.

30/3,AB/18 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03480045
SEMICONDUCTOR WAFER

PUB. NO.: 03-142945 [JP 3142945 A]
PUBLISHED: June 18, 1991 (19910618)
INVENTOR(s): TOYODA HIROYUKI
APPLICANT(s): NEC KANSAI LTD [485545] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-282427 [JP 89282427]
FILED: October 30, 1989 (19891030)
JOURNAL: Section: E, Section No. 1111, Vol. 15, No. 365, Pg. 55, September 13, 1991 (19910913)

ABSTRACT

PURPOSE: To prevent the quality degradation of non-defective **chip** by marking, enable automatic selection, and facilitate matching between a wafer and recorded contents, by arranging a **chip** for recording whether an element is non-defective, on a semiconductor wafer, independently of product **chips**.

CONSTITUTION: Product **chips** 2 are formed on a wafer 1 so as to interpose scribe lines 3, and a **chip** 4 for recording whether an element is non-defective is formed. A pattern 9 of the same arrangement as that of product **chips** on the wafer is formed on the **chip** 4. The pattern 9 is constituted of a metal **electrode** 6, an **insulating film** 7, and a wafer substrate 8, and the record concerning to whether an element is non-defective is formed upon whether it marks the trace of a **probe** on the metal **electrode** 6, or **breaks** down the **insulating film** by applying an excess voltage on the metal **electrode** 6. The contents recorded in the above manner are clear because there is no influence of a substratum pattern and unevenness, and can be easily read optically or electrically in the later process. Thereby a defect mark can be clearly recorded, and the matching between the wafer and the recorded contents concerning to whether an element is non-defective can be facilitated.

30/3,AB/19 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02881828
MEASUREMENT OF **INTEGRATED CIRCUIT**

PUB. NO.: 01-179428 [JP 1179428 A]
PUBLISHED: July 17, 1989 (19890717)
INVENTOR(s): AMANO NOBUTAKA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-002304 [JP 882304]
FILED: January 07, 1988 (19880107)
JOURNAL: Section: E, Section No. 832, Vol. 13, No. 459, Pg. 160, October 17, 1989 (19891017)

ABSTRACT

PURPOSE: To bring the **probes** into good contact with **pads** thereby stabilizing the yield by inspecting wafers by a method wherein a voltage is impressed between **pads** of an **IC** to supply them with current for **breaking** down thin **insulating films** on the **pad** surfaces.

CONSTITUTION: Within an ordinary **IC**, excluding power supply **pads**, a static breakdown preventive diode 8 is connected to a vCC terminal and a GND terminal. A GND **pad** 6 is impressed with positive voltage to supply another **pad** 7 with GND potential. Then, the **pads** 6, 7 are supplied with current through the diode 8 **breaking** down thin **insulating films** 4 to bring **probes** 1, 2 into good contact respectively with the **pads** 7, 6. Later, the yield can be prevented from deteriorating due to any defective contact by inspecting the electrical properties of the **IC**.

30/3,AB/20 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02750436
METHOD FOR CORRECTING ACTIVE MATRIX ARRAY

PUB. NO.: 01-048036 [JP 1048036 A]
PUBLISHED: February 22, 1989 (19890222)
INVENTOR(s): TAKAHARA HIROSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-204641 [JP 87204641]
FILED: August 18, 1987 (19870818)
JOURNAL: Section: P, Section No. 881, Vol. 13, No. 245, Pg. 137, June 08, 1989 (19890608)

ABSTRACT

PURPOSE: To correct an active matrix array by disconnecting a defective thin film transistor TFT from the 1st picture element **electrode** and impressing a voltage between the 2nd picture element **electrode** adjacent to said **electrode** and the conductive connecting wiring thereby inducing **dielectric breakdown** between the connecting wiring and the 2nd **electrode** and connecting the picture element **electrodes** when the defective TFT arises in the above-mentioned array.

CONSTITUTION: The 1st picture element **electrode** 1a is formed to the active matrix array and the 2nd picture element **electrode** 1c adjacent to the **electrode** 1a is electrically connected via an **insulator film**. A 1st electrical connecting means (**probe**) 16 is brought into pressurized contact with the surface of the conductive connecting wiring 14 superposed perpendicularly on this **electrode** 1c to deform the wiring 14. A 2nd **probe** 17 is brought into pressurized contact with the **electrode** 1c and the voltage is impressed between the **probes** 16 and 17 by a voltage impressing means 18 via a switch 19. The **dielectric breakdown** is generated in the **insulator film** 2 and the **electrodes** 1a and 1c are electrically connected. The correction of the defect is thus executed at a low cost.

30/3,AB/21 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01930759
MANUFACTURE OF SEMICONDUCTOR **IC** DEVICE

PUB. NO.: 61-144859 [JP 61144859 A]
PUBLISHED: July 02, 1986 (19860702)
INVENTOR(s): ASANO SHINJI
ITO TSUNEO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-266157 [JP 84266157]
FILED: December 19, 1984 (19841219)
JOURNAL: Section: E, Section No. 455, Vol. 10, No. 340, Pg. 152, November 18, 1986 (19861118)

ABSTRACT

PURPOSE: To obtain highly reliable result of test by a method wherein **dielectric breakdown** strength test of a gate **insulated film** using a gate **electrode** which is formed into plural MISFET gate **electrodes** in one body.

CONSTITUTION: An Si oxide film is formed on the surface of a semiconductor substrate 2. Thereafter, a field **insulated film** 9 is formed on the prescribed surface of the substrate 2. After that, a gate **insulated film** 10 is formed after the surface of the substrate 2 is oxisized, then plural gate **electrodes** 11 are formed in one body. The end sections of the **electrodes** 11 are extended horizontally to the periphery secton of the substrate 2, and the said end sections are formed at an bonding-**pad** state **electrode** 12. Then, the **electrode** 11 and the substrate 12 are subjected to high voltage and low voltage respectively by connecting electri- cally the **probe** of a tester with the substrate 12, and voltage is impessed between 11 and 12, thus **dielectric breakdown** strength of the film 10 is measured. Consequently, it is separated electrically between the **electrode** 11 and 12. In this manner, highly reliable result of test is obtained because sum total area of the film 10 below the **electrode** 11 installed at a basic cell row occupies almost whole area of the film 10 on the surface of the **chip**.

30/3,AB/22 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01918782
DIELECTRIC BREAKDOWN RATING EVALUATING METHOD AND ITS DEVICE

PUB. NO.: 61-132882 [JP 61132882 A]
PUBLISHED: June 20, 1986 (19860620)
INVENTOR(s): ISHIDA TOSHIHARU
YOSHIDA TORU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-253999 [JP 84253999]
FILED: December 03, 1984 (19841203)
JOURNAL: Section: P, Section No. 512, Vol. 10, No. 324, Pg. 164, November 05, 1986 (19861105)

ABSTRACT

PURPOSE: To non-destructively decide the quality of a thin film based on a current deviation by applying simultaneously the same pulse voltage of an extent that a **dielectric breakdown** is not generated, to an **insulating** thin **film** and a reference capacity having a capacity corresponding to a capacity of said thin film, and comparing transient currents.

CONSTITUTION: A sample to be inspected 1 is formed by placing a gate isulating thin film 3 on a p type silicon semiconductor element substrate 2, and a polysilicon film **electrode** 4 on said film respectively. In this state, to the sample 1, a pulse voltage is applied from a pulse generating means 7 through a **probing** means 6, and this pulse voltage is applied simultaneously to a reference capacity 5, too. When this pulse voltage is applied, a voltage corresponding to a transient current waveform is generated from resistances 8, 9. Also, based on a voltage from the resistance 8 as a reference, a deviation value of a voltage from the resistance 9 is derived by a voltage deviation detecting means 10, sampled by a gate means 11 by a sampling pulse from the means 7, and compared with a reference voltage corresponding to the sampling time point. In this way,

the quality of the thin film of every sampling time point can be decided.

30/3,AB/23 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01874439
MOS FIELD EFFECT TRANSISTOR

PUB. NO.: 61-088539 [JP 61088539 A]
PUBLISHED: May 06, 1986 (19860506)
INVENTOR(s): KANAMORI SHUJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-210704 [JP 84210704]
FILED: October 08, 1984 (19841008)
JOURNAL: Section: E, Section No. 435, Vol. 10, No. 263, Pg. 49, September 09, 1986 (19860909)

ABSTRACT

PURPOSE: To realize estimation of strength of element portion by providing both similar pseudo gate **insulating film** and pseudo gate **electrode** on the same substrate and applying a voltage through a **probe** applied to the **electrode** located on a thick film on the occasion of forming MOSFET through attachment of gate **electrode** on a thin gate **insulating film** surrounded by a thick **insulation film**.

CONSTITUTION: A gate **insulating film** surrounded by a thick **insulating film** is formed on a semiconductor substrate and the region from gate insulating **film** to thick **insulating film** is covered with gate **electrode** to form a MOSFET. In such a structure, a thick external **insulating film** 8 in the same shape, a pseudo gate **insulating film** 14 surrounded by said film and pseudo gate **electrode** 15 which is extending onto the film 8 and comprising the stepped portion 10 are provided on the same substrate 1, a **probe** 9 is applied to the **electrode** 9 on the stepped portion 10 and a voltage is applied to such **probe** and it is gradually raised. The breakdown strength of element portion can be estimated from **breakdown** of **insulating film** 14 thus generated in order to realize quality control in the manufacturing process.

30/3,AB/24 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

01292343
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 59-003943 [JP 59003943 A]
PUBLISHED: January 10, 1984 (19840110)
INVENTOR(s): IWAZAWA SHIGEO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-113692 [JP 82113692]
FILED: June 29, 1982 (19820629)

JOURNAL: Section: E, Section No. 238, Vol. 08, No. 81, Pg. 134, April 13, 1984 (19840413)

ABSTRACT

PURPOSE: To enhance assembling and manufacturing yield of the semiconductor device by a method wherein an **insulating** resin **film** is formed on the surface of a semiconductor wafer, and a **probe** is made to come in contact with an **electrode** **breaking** through the **insulating** resin **film** thereof to perform a **probe** test.

CONSTITUTION: A polyvinyl alcohol liquid is jetted with a spray on the semiconductor wafer 11 (containing the **electrode** 3 and regions 1, 2) formed with a high voltage semiconductor element, the volatile matter of alcohol, etc., are evaporated, and the PVA film 12 is coveringly formed. After the whole surface of the semiconductor wafer 11 is protected completely with the PVA film 12, a **probe** 13 is made to come in contact with the **electrode** at the **probe** test. The **electrode** can be confirmed favorably because the PVA film 12 is transparent, and because the film is very soft, the **probe** 13 can be made to come in contact with the base **electrode** 3, etc., breaking through the film with the tip thereof to hold ohmic contact. Quality of the semiconductor element is discriminated thereby, and after a red mark, for example, is adhered to an inferior goods, dicing is performed with a dicing tool 14.

33/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6852832 INSPEC Abstract Number: B2001-04-2180-001
Title: Resistance change at copper contacts with thin and thick oxide films under a zero force liquid gallium probe
Author(s): Liu, D.R.; McCarthy, S.
Author Affiliation: Sci. Res. Lab., Ford Motor Co., Dearborn, MI, USA
Conference Title: Electrical Contacts - 2000. Proceedings of the Forty-Sixth IEEE Holm Conference on Electrical Contacts (Cat. No.00CB37081) p.183-9
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xvi+279 pp.
ISBN: 0 7803 5960 7 Material Identity Number: XX-2000-02757
U.S. Copyright Clearance Center Code: 0 7803 5960 7/2000/$10.00
Conference Title: Electrical Contacts - 2000. Proceedings of the Forty-Sixth IEEE Holm Conference on Electrical Contacts
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE
Conference Date: 25-27 Sept. 2000 Conference Location: Chicago, IL, USA
Language: English
Abstract: Experiments were performed to investigate the contact resistance behavior and breakdown characteristics of the oxidized copper surface. In order to eliminate the influence of the mechanical pressure on the contact resistance, a gallium liquid metal drop was used as the probe. Current was varied from 0.1 mA to 1 A and then ramped back down to 0.1 mA. The voltage across the contact between a gallium drop and the oxidized copper was recorded. The contact resistance was then computed and plotted against the voltage. It was discovered that the A-**fritting** voltage of the contact was about 2.0 V when the film thickness was about 55 nm, which was consistent with the results of Holm (1967). It was also observed that the film could break down and then recover partially for several cycles before the film was finally broken down completely to settle at a lower voltage. When the film thickness was 8 nm or less, the measured contact voltage at the **fritting** stage was always less than 0.4 V. In such cases, it was not possible to observe the typical `avalanche' A-**fritting** (breakdown), even though the film had not been ruptured by mechanical load.
Subfile: B

33/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03931535 INSPEC Abstract Number: B91049299
Title: Conduction in failing aluminum connections
Author(s): Aronstien, J.
Author Affiliation: Protune Corp., Poughkeepsie, NY, USA
Journal: IEEE Transactions on Components, Hybrids, and Manufacturing Technology vol.14, no.1 p.170-5
Publication Date: March 1991 Country of Publication: USA
CODEN: ITTEDR ISSN: 0148-6411
U.S. Copyright Clearance Center Code: 0148-6411/91/0300-0170$0.1.00
Conference Title: 1990 36th IEEE Holm Conference on Electrical Contacts

and the 15th International Conference on Electric Contacts
Conference Sponsor: IEEE; Canadian Electr. Assoc
Conference Date: 20-24 Aug. 1990 Conference Location: Montreal, Que., Canada
Language: English
Abstract: Conduction in failing aluminum contacts was studied using oscilloscope observation of the current-voltage characteristics. Crossed wire and twisted pair contacts are used in these studies. The dual crossed wire configuration permits evaluation of the distribution of the conducting channels. Measurement of contact resistance as normal force is increased shows that there is little metallic contact established through the aluminum oxide by application of normal force alone. Conduction in these aluminum connections is found to be predominantly metallic, however, established and sustained by the electrical breakdown mechanism known as A-**fritting** . The metallic conductive channels formed by this mechanism deteriorate and open, causing frequent repetition of the breakdown process. The results indicate that there is likely to be only one conducting channel active at a time. Observations made on aluminum-aluminum twisted pair and twist-on connector splices demonstrate that the same mechanism is operative for these connections. The relationship of the results to behavior of failing aluminum connections is discussed.
Subfile: B

33/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

00867756 INSPEC Abstract Number: B76008547
Title: Electroforming or **fritting** in surface films on contacts
Author(s): Guile, A.E.; Morgan, D.V.
Author Affiliation: Dept. of Electrical & Electronic Engng., Univ. of Leeds, Leeds, UK
Journal: Proceedings of the Institution of Electrical Engineers vol.122, no.12 p.1454-5
Publication Date: Dec. 1975 Country of Publication: UK
CODEN: PIEEAH ISSN: 0020-3270
Language: English
Abstract: Attention is drawn to the similarities between 'electroforming' or 'switching' processes by which the film of 10-2000 nm in thickness changes from low conductivity to high conductivity, and '**fritting**' processes by which oxide or other films become conducting which do not involve electron avalanches.
Subfile: B

33/3,AB/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00068033
E.I. Monthly No: EI70X011885
Title: Tarnishing and contamination of metals.
Author: CAMPBELL, W. E.; THOMAS, U. B.
Corporate Source: Rensselaer Polytechnic Inst, Troy, NY
Source: Illinois Inst of Technology-Proc of Holm Seminar on Electric Contact Phenomena Nov 11-15 1968 p 233-63
Publication Year: 1968

Language: ENGLISH
Abstract: If voltage across contact at make or break is less then lowest **fritting** voltages which have been encountered experimentally, that is, less than 0. 03 v, problems in reliabilty are greatly increased; contacts operating in this manner are concern of this report; under these conditions it is possible for **insulating films** to build up to thickness sufficient to cause serious contact noise as well as to cause failure by open circuit; contaminants found on electrical contacts are described.

33/3,AB/5 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03005452 JICST ACCESSION NUMBER: 96A0652340 FILE SEGMENT: JICST-E
Tribology in current flow. Tribology in Sliding Contacts.
WATANABE YOSHITADA (1)
(1) Kogakuin Univ., Fac. of Eng.
Toraiborojisuto(Journal of Japanese Society of Tribologists), 1996, VOL.41,NO.7, PAGE.552-557, FIG.11, REF.22
JOURNAL NUMBER: F0390ABW ISSN NO: 0915-1168 CODEN: TORAE
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.066
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: As sliding contacts are miniaturized and low powered, tribology phenomena are made clear. The results of experiments are shown and the problems and solutions are described. Noise is caused by the instantaneous change of contact resistance and arc discharge. **Fritting** by which **insulation film** is electrically broken does not occur in small power and the contact is stabilized by increasing the current and breaking the film with Joule heat. Lubrication is effective and therefore a contact material with solid lubricant mixed, the application of lubricating oil and vapor lubrication are developed.

33/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013897934
WPI Acc No: 2001-382147/200141
XRPX Acc No: N01-280262
Plasma display **apparatus** includes **frit** glass layer provided between front glass substrate and barrier plate
Patent Assignee: SAMSUNG SDI CO LTD (SMSU); SAMSUNG DENKAN KK (SMSU)
Inventor: HWANG H Y; KIM M S; PARK D I; RYU C Y; RYOO C Y
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CN 1279498	A	20010110	CN 2000118492	A	20000531	200141	B
JP 2001035396	A	20010209	JP 2000199020	A	20000630	200164	
KR 2001008625	A	20010205	KR 9926545	A	19990702	200152	
KR 342047	B	20020627	KR 9926545	A	19990702	200282	

Priority Applications (No Type Date): KR 9926545 A 19990702
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CN 1279498	A			H01J-017/49	
JP 2001035396	A		5	H01J-011/02	
KR 2001008625	A			H01J-017/49	
KR 342047	B			H01J-017/49	Previous Publ. patent KR 2001008625

Abstract (Basic): JP 2001035396 A
Abstract (Basic):

NOVELTY - A **dielectric layer** (24) is provided on the inner surface of a front glass substrate (21) and a back glass substrate (22), covering display and address electrodes. A barrier plate (27) is provided on layer (24) of substrate (22). A frit glass layer (31) is provided between substrate (21) and upper surface of plate (27), so that heating fusion of the substrates is done to upper portion of plate (27).

DETAILED DESCRIPTION - The front and back glass substrate are positioned mutually opposite, are joined. The strip-shaped display electrode and address electrode are formed on the inner surface of the front and back substrates, in mutually perpendicular direction. The width of the frit glass layer is 10-100% of the width of the barrier plate upper surface and thickness is 1 or 50 mum, after sealing the front and back substrates. An INDEPENDENT CLAIM is also included for plasma display apparatus manufacturing method.

USE - Plasma display apparatus.

ADVANTAGE - Avoids detachment of the front substrate from the barrier plate under low pressure. Withstands injection of discharge gas at high pressure, thus improving discharge efficiency. Prevents deformation of the substrate by heat. Enables enlargement of a screen by using substrate of large area.

DESCRIPTION OF DRAWING(S) - The figure shows the exploded perspective view of the plasma display apparatus.

Front, back glass substrates (21,22)
Dielectric layer (24)
Barrier plate (27)
Frit glass layer (31)
pp; 5 DwgNo 2/2

33/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013394745
WPI Acc No: 2000-566683/200053
XRAM Acc No: C00-168970
XRPX Acc No: N00-418594
Photosensitive **insulating** paste for thick **film** multilayer circuit substrates with small via holes high Q value and a low relative dielectric constant comprising a borosilicate glass and crystalline silicon oxide
Patent Assignee: MURATA MFG CO LTD (MURA)
Inventor: KAWAKAMI H; TOSE M; WATANABE S
Number of Countries: 028 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1029829	A1	20000823	EP 2000101701	A	20000127	200053	B

JP 2000243137	A	20000908	JP 9938762	A	19990217	200058	
CN 1264131	A	20000823	CN 2000102332	A	20000216	200063	
US 20020035194	A1	20020321	US 2000496159	A	20000201	200224	
			US 2001915704	A	20010726		
US 6403694	B1	20020611	US 2000496159	A	20000201	200244	
US 6602946	B2	20030805	US 2000496159	A	20000201	200353	
			US 2001915704	A	20010726		

Priority Applications (No Type Date): JP 9938762 A 19990217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1029829	A1	E	24	C03C-008/16	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000243137	A		14	H01B-003/08	
CN 1264131	A			H01B-003/00	
US 20020035194	A1			B32B-017/06	Div ex application US 2000496159
US 6403694	B1			C08K-003/34	
US 6602946	B2			C08K-003/34	Div ex application US 2000496159 Div ex patent US 6403694

Abstract (Basic): EP 1029829 A1
Abstract (Basic):

NOVELTY - The insulating paste comprises a photosensitive binder and borosilicate glass and crystalline silicon dioxide mixed in a compositional proportion within a defined region in a ternary diagram. Both powders have define particle size and shape-smoothness index.

DETAILED DESCRIPTION - Photosensitive insulating paste comprising a borosilicate glass powder and a crystalline silicon oxide SiO2 powder in an amount to give 3 - 40 wt% after sintering, all dispersed in a photosensitive organic vehicle. INDEPENDENT CLAIMs are also included for thick film multilayer circuit substrate comprising the combination of an insulating substrate and an **insulating layer** formed by screen printing followed by exposure, development and sintering of the claimed pastes.

USE - High frequency circuits, and thick film multilayer circuit substrates.

ADVANTAGE - The **insulating layer** has a high Q value and a low relative dielectric constant in good balance, and improved via holes may be formed at increased density.

DESCRIPTION OF DRAWING(S) - The drawing shows a ternary diagram showing a compositional region of a borosilicate glass powder contained in a photosensitive insulating paste.

pp; 24 DwgNo 1/4

33/3,AB/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008005429
WPI Acc No: 1989-270541/198937
XRPX Acc No: N89-206558
Fritting technique for audio circuit switches - applying voltage across switch terminals to provide high current that breaks down **insulating layer**
Patent Assignee: LINDSAY AUDIOPHYLE (LIND-N)
Inventor: LINDSAY-GEYER D S

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4851707	A	19890725	US 8774382	A	19870716	198937	B

Priority Applications (No Type Date): US 8774382 A 19870716
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4851707	A		5		

Abstract (Basic): US 4851707 A

Conductive leads (26, 28) connect to the batteries (24) and extend to the surface (22a) of the case (22). Jacks (30, 32) are provided at these points to receive the ends of respective clip leads (34, 36) whose other ends can appropriately be attached to the leads (10, 12) respectively. An indicator light (38) is included in the lead. In use, with the inclusion of the clip leads the clips are attached to the leads and voltage from the batteries is applied across the pair of contacts when they are adjacent each other, i.e. with the switch (14) closed, to provide current through the contacts. This current is chosen to be substantially greater than the current carried through the contacts during their normal use in the audio system. In fact, it has been found advantageous to provide a current of at least 0.5 amperes through the contacts with the voltage determining this current being applied for at least 0.5 seconds.

This process acts to remove the **insulating** oxide **layers** as described above through the technique of fitting.

ADVANTAGE - Greatly increases sound quality of system in which **insulating** oxide **layer** of any substance has been allowed to build up on the contacts.

1/2

33/3,AB/9 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007452352
WPI Acc No: 1988-086286/198813
XRAM Acc No: C88-038667
XRPX Acc No: N88-065138
Neodymium titanate-based type 1 dielectric compsn. - used for multilayer capacitors, contains lead titanate, barium titanate, barium zirconate and yttrium oxide
Patent Assignee: LCC-CICE CIE EURO COMPOSANTS (LCCC)
Inventor: BEAUGER A; ROSSELLO A; SCHNEIDER C
Number of Countries: 006 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 262041	A	19880330	EP 87402102	A	19870921	198813	B
FR 2604429	A	19880401	FR 8613484	A	19860926	198820	
US 4769354	A	19880906	US 87101781	A	19870928	198838	

Priority Applications (No Type Date): FR 8613484 A 19860926
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 262041	A	F	6		

Designated States (Regional): DE GB IT NL

US 4769354 A 3

Abstract (Basic): EP 262041 A

A type 1 dielectric compsn. consists of a mixt. of (by wt.) 58-70% neodymium titanate, 10-21% lead titanate, 5-14% barium titanate, 4-15 (e.g. 10.7)% barium zirconate and 0.2-1.2 (e.g. 0.97)% yttrium oxide.

USE/ADVANTAGE - The dielectric compsn. is useful for multilayer ceramic capacitors. It has a sintering temp. of 1280-1300 deg.C (allowing use of electrodes of 70 wt.% Pd/30 wt.% Ag alloy) and, at 1 MHz frequency, a dielectric constant of 75-85, an h.f. stable loss angle tangent of 4-8 x 10 power-4 and a temp. coefficient of 0 +/- 30 ppm corresponding to NPO class.

In an example, 50-60g powder, of compsn. 64.0% neodymium titanate, 11.65% lead titanate, 12.62% barium titanate, 10.68% barium zirconate and 0.97% yttrium oxide, was mixed with 100cc. deionised water in a polyethylene vessel contg. 200g zirconia balls for 2 hrs.. After binder addn., the resulting slurry was dried to powder and sieved. The powder was pressed to 1mm-thick, 8.4mm diameter discs and sintered in an oxidising atmos. at 1280-1300 deg.C. After deposition of silver electrodes, the resulting capacitors had a density of 5.49, a dielectric constant (20 deg.C, 1 MHz) of 77.6, a loss factor (tan delta at 20 deg.C) of 4 x 10 power (-4) at 1 MHz, 12 x 10 power (-4) at 1 kHz and 10 x 10 power (-4) at 100 Hz, and a temp. coefficient of (-)4.

0/0

Abstract (Equivalent): US 4769354 A

Type I dielectric compsn., i.e. having low dielectric cosntant between 10 and 90, consists of (wt.%) 58-70 Nd titanate, 10-21 Pb titanate, 5-14 pref. 10.7 Ba titanate, 4-15 Ba zirconate, and 0.2-1.2, pref. 0.97 Y oxide. The compsns. have **fritting** temps. of 1280-1300 deg.C, allowing the use of 70% Pd - 30% Ag alloy electrodes in mfr. of **multi-layered** capacitors. **Dielectric** constant ranges from 75-85 with loss factors of 4-8 x 10 power -4, stable at high frequencies. Temp. coefft. varies from 0 to +/- 30. ADVANTAGE - Type 1 performance is maintained while allowing **fritting** at high temps.

(3pp

33/3,AB/10 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004327819
WPI Acc No: 1985-154697/198526
XRPX Acc No: N85-116814
Radiation-hard multi-layer ceramic capacitor - has ceramic capping layers with high proportion of low-atomic-mass elements and low dielectric strength
Patent Assignee: EUROFARAD-EFD (EURO-N)
Inventor: DUBUISSON J; GAL P L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2555355	A	19850524	FR 8318572	A	19831122	198526	B

Priority Applications (No Type Date): FR 8318572 A 19831122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

FR 2555355 A 7

Abstract (Basic): FR 2555355 A

The capacitor has alternate conducting layers are connected to a common metallised walls (13,14) of the capacitor block (10). Additional **dielectric** capping **layers** (20,20') are incorporated into the upper and lower faces of the block.

The capping layers are made of a low dielectric strength ceramic containing a high concentration of light-atom species. These lamps protect the body of the capacitor from incoming radiation. The capping-layer ceramic is based on magnesium titanate with zinc, zirconium and calcium oxides added. The ceramic types used for capping and inner layers are chosen to be compatible in their **fritting** temperatures, shrinkage coefficients and mutual diffusion coefficients. The **dielectric** constant of capping **layers** is typically one tenth of that of the internal capacitor dielectric, ie the strength of the latter, is greater than 1000, and the former less than 100.

1/1

33/3,AB/11 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003655238
WPI Acc No: 1983-15218K/198307
XRAM Acc No: C83-014795
XRPX Acc No: N83-028349
Fluid-tight negative terminal feedthrough for lithium battery - with oxide coating on terminal post surrounded by glass
Patent Assignee: GIPELEC SA (GIPE-N)
Inventor: CHENAUX B
Number of Countries: 015 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 71094	A	19830209				198307	B
FR 2510310	A	19830128				198310	
JP 58025076	A	19830215				198312	
US 4438184	A	19840320	US 82397436	A	19820712	198414	
CA 1196054	A	19851029				198548	
IL 66370	A	19851129				198602	

Priority Applications (No Type Date): FR 8114151 A 19810721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 71094	A	F	6		

Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE

Abstract (Basic): EP 71094 A

The negative terminal is a tubular post (1) of e.g. stainless steel, Fe-Ni or Fe-Cr alloy, titanium or tantalum projecting through a metallic shell (2) connected to the positive pole. A glass seal (3) surrounds the post (1) which is coated (e.g. by plasma spraying) on its external surface with a **layer** (4) of **insulating** oxide (e.g. alumina) whose thickness may vary between a few microns and a few tenths of a millimetre.

The coating may be treated e.g. by **fritting** at 1500-1800 deg.C to reduce its porosity. Alternatively a titanium post may be

coated by anodic oxidation. After coating, the post is fixed in position by conventional compression sealing with glass fusion.
Device is esp. incorporated in a cell.
1/1

33/3,AB/12 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003364678
WPI Acc No: 1982-M2704E/198237
Surface acoustic wave converter mfr. - by using ionisation radiation interaction on piezoelectric plate to form **dielectric coating**
Patent Assignee: LENGD AVIATION INST (LEAU)
Inventor: CHALABYAN G A; PIROGOV B N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 881980	B	19811115				198237	B

Priority Applications (No Type Date): SU 2884864 A 19800214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 881980	B		4		

Abstract (Basic): SU 881980 B
Signals processing equipment surface acoustic wave converter mfr. has simplified mfg technology and the converter has improved resistance to temp. drops achieved by forming the **dielectric coating** on the piezoelectric plate by means of interaction of ionising radiation on the plate with the radiation doses sufficient to amorphosise the plate's surface **layer**. The **dielectric coating** is formed by the photolithography method.
Initially, the piezoelectric plate is cleaned and placed in the ionising radiation appts. (radiation circuit of a reactor, gamma-appts, accelerator etc); the amorphous layer is formed over the entire working surface of the plate (1).
The photoresist is then applied by the photolithography process, followed by exposure through masks using uv light etc. In as much as the amorphous layer is formed in the body of the actual plate (1) then good adhesion takes place and matching of the temp. coeffts. of expansion of the layer and plate. Thus **fritting** and cracking of the **dielectric layer** is avoided during mfr. and use of the converter. Bul.42/15.11.81 (4pp)

33/3,AB/13 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003075416
WPI Acc No: 1981-H5455D/198133
Aquarium immersion heater with particulate electrical resistor - is coated with waterproof mouldable resinous thermally conducting material which is safeguarded against overheating
Patent Assignee: GLORIA SA (GLOR-N)
Inventor: DUMAS J C

Number of Countries: 013 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 33278	A	19810805				198133	B
FR 2474802	A	19810731				198136	
US 4354096	A	19821012				198243	
CA 1173885	A	19840904				198440	

Priority Applications (No Type Date): FR 801875 A 19800129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 33278	A	F	11		

Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE

Abstract (Basic): EP 33278 A

The resistor consists of e.g. metallic or carbon particles dispersed within a hydrocarbon polymer matrix and is made by conventional processes, e.g. **fritting**, and heated to a temp. which is sufficient for controlled destruction of the polymer to establish the desired value of resistance. The coating may be an epoxide, polyurethane or polyester resin loaded with e.g. metal oxides for thermal conductivity.

A device may be incorporated to measure the internal or external temp. of the resistor or to ascertain the presence of surrounding water. There is also provided electronic control which is responsive to the difference between actual and desired or max. admissible temps. The conventional thermally **insulating** air **film** and fragile glass envelope around the resistor are eliminated. The device can be a thin plate placed against the aquarium wall, or be shaped to simulate an ornamental underwater rock.

33/3,AB/14 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

000560736
WPI Acc No: 1968-01557Q/196800
Moulded cellular objects from ethylene-acrylate
Patent Assignee: BADISCHE ANILIN & SODA FAB AG (BADI)
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
BE 703627	A					196800	B
AU 6726659	A					196801	
FR 1536092	A					196801	
NL 6712229	A					196801	
GB 1190457	A					197018	
CA 860835	A					197103	
JP 71035993	B					197142	
DE 1669663	A	19720302				198536	

Priority Applications (No Type Date): DE B88837 A 19660909

Abstract (Basic): BE 703627 A

Moulded cellular articles are produced by heating in a closed mould, with **fritting**, cellular particles of ethylene copolymers which include carboxylic acid groups and groups derived from t-butyl or isopropyl esters of carboxylic acids.

Mouldings of complicated shape can be produced.
The cellular products may be used as stuffings, packings, heat- and sound-**insulation**, floating lids, **films** or bands.

33/3,AB/15 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07271079
INSPECTION METHOD AND INSPECTION DEVICE

PUB. NO.: 2002-139542 [JP 2002139542 A]
PUBLISHED: May 17, 2002 (20020517)
INVENTOR(s): IINO SHINJI
TAKEKOSHI KIYOSHI
SUGA TADATOMO
ITO HISAHIRO
KATAOKA KENICHI
APPLICANT(s): TOKYO ELECTRON LTD
SUGA TADATOMO
ITO HISAHIRO
APPL. NO.: 2001-093303 [JP 20011093303]
FILED: March 28, 2001 (20010328)
PRIORITY: 2000-249702 [JP 2000249702], JP (Japan), August 21, 2000 (20000821)

ABSTRACT

PROBLEM TO BE SOLVED: To solve such problems in an inspection method that the service life of a probe N is shortened by scrubbing and that yield of a device is reduced by damaging the inspection electrode P as shown in (b) of figure 7 when the probe N is brought into contact with an inspection electrode P electrically by scrubbing operation.

SOLUTION: This inspection method for executing electric characteristic inspection of the device by bringing an inspection probe 12A into electric contact with the inspection electrode P, has a contact process for bringing the inspection probe 12A into electric contact with the inspection electrode P by breaking an **insulating coat** O of the inspection electrode P by utilizing **fritting phenomenon**.

36/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

01117460 INSPEC Abstract Number: B77041859
Title: Stable Josephson junctions fabricated by **fritting**
Author(s): Bondarenko, S.I.; Matveeva, V.A.; Loboda, N.M.; Loganov, K.B.; Shul'man, A.S.
Author Affiliation: Physicotech. Inst. of Low Temperatures, Acad. of Sci., Khar'kov, Ukrainian SSR, USSR
Journal: Zhurnal Tekhnicheskoi Fiziki vol.46, no.11 p.2440-3
Publication Date: Nov. 1976 Country of Publication: USSR
CODEN: ZTEFA3 ISSN: 0044-4642
Translated in: Soviet Physics - Technical Physics vol.21, no.11 p. 1440-2
Publication Date: Nov. 1976 Country of Publication: USA
CODEN: SPTPA3 ISSN: 0038-5662
Language: English
Abstract: Experiments are reported on the development of regular weak links, which can be called 'superconducting microbridges' fabricated by the controlled **dielectric breakdown** method (**fritting**). These bridges withstand repeated temperature cycling and preserve their characteristics after several months storage at room temperature.
Subfile: B

36/3,AB/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00352393
E.I. Monthly No: EI7403015456
Title: NOTE ON THE OXIDATION PROPERTIES OF BINARY ALLOYS OF RHENIUM WITH TUNGSTEN, MOLYBDENUM, PALLADIUM AND RUTHENIUM.
Author: Lindborg, U.; Ronnquist, A.
Corporate Source: Jernkontoret Res Organ, Stockholm, Swed
Source: Scandinavian Journal of Metallurgy v 2 n 5 1973 p 242
Publication Year: 1973
CODEN: SJMLAG ISSN: 0371-0459
Language: ENGLISH
Abstract: The oxidation properties of a number of rhenium alloys have been studied for a rough first evaluation of their potential as materials for electrical contacts. The corrosion layers which formed were on most occasions insulating. The technically most relevant property is the so-called **fritting** voltage required to **break** through the **insulation**. The **fritting** voltage always shows large scatter. In some cases the contact resistance could be measured without **fritting**. For the thicker oxide layers obtained at 450 DEGREE C attempts were made to identify the products by means of an X-ray diffractometer. 1 ref.

43/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06282462
E.I. No: EIP03047340255
Title: Electroplating Ni micro-cantilevers for low contact-force **IC probing**
Author: Kataoka, Kenichi; Kawamura, Shingo; Itoh, Toshihiro; Ishikawa, Kaoru; Honma, Hideo; Suga, Tadatomo
Corporate Source: Res. Ctr. for Adv. Sci. and Technol. University of Tokyo, Tokyo 153-8904, Japan
Source: Sensors and Actuators, A: Physical v 103 n 1-2 Jan 15 2003. p 116-121
Publication Year: 2003
CODEN: SAAPEB ISSN: 0924-4247
Language: English
Abstract: We present a new MEMS **probe** card made of electroplated nickel micro-cantilevers, which has compliant structures, and uses a kind of electric breakdown, or **fritting**, to make electric contacts to **electrodes** on ICs. The characteristics of **fritting** contact between nickel **probe** and Al **electrodes** were investigated, and nickel was found to have lower contact resistance than other materials. A micro-machining process for the **probe** cards, including deposition of layers having different internal stress to make a protruding cantilever shape, was developed. It was found that the **fritting** process using the micro-cantilevers could make the low-resistance contacts with the force of less than a few micronewtons. copy 2003 Elsevier Science B.V. All rights reserved. 10 Refs.

43/3,AB/2 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

01394232 PASCAL No.: 77-0013439
RESULTS OF A 160 X 10 SUP 6 DEVICE-HOUR RELIABILITY ASSESSMENT AND FAILURE **ANALYSIS** OF TTL SSI **INTEGRATED CIRCUITS**. II. SURVEY OF DOMINANT **IC** FAILURE MECHANISMS AND **ANALYSIS** OF FAILURE CAUSES.
KEMENY A P; KALMAR G; STEFANIAY V
IND. RES. INST. ELECTRON. HIKI, BUDAPEST,HUNGARY
Journal: MICROELECTRON. AND RELIABIL., 1975, 14 (5-6) 499-526 25
Language: ENGLISH
ON ETUDIE LES PLUS IMPORTANTS MECANISMES DE DEFAILLANCES DES CIRCUITS INTEGRES MONOLITHIQUES COMME PAR EXEMPLE LES DEFAUTS DE LIAISONS ET DE TROUS, LES DEFAILLANCES DE LA METALLISATION, COMME LES REACTIONS AL-SI ET LA FORMATION DE CAVITES DE **FRITTAGE**, AINSI QUE LES **PHENOMENES** DE TRANSPORT DE MASSE, C'EST-A-DIRE LA THERMOMIGRATION ET L'ELECTROMIGRATION, UNE CORROSION TRES PRONONCEE ET CERTAINS PROBLEMES RELIES AU MONTAGE ET A L'ENCAPSULAGE; TOUT CECI PROVOQUE UNE USURE PREMATUREE ET UN RACCOURCISSEMENT DE LA DUREE DE VIE DES CIRCUITS INTEGRES. LES EXPLICATIONS DES MECANISMES DE DEFAILLANCES SONT ECLAIREES PAR DES MICROGRAPHIQUES, OBTENUS GRACE AU MICROSCOPE ELECTRONIQUE, ET PORTANT SUR DES DISPOSITIFS DEFAILLANTS.

43/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014507939
WPI Acc No: 2002-328642/200236
XRPX Acc No: N02-257899
Semiconductor device inspection method for measuring electrical characteristics, involves applying a voltage between two **probes** in contact with oxide film to induce **fritting** and breakage of film
Patent Assignee: ITOH T (ITOH-I); SUGA T (SUGA-I); TOKYO ELECTRON LTD (TKEL); ITO K (ITOK-I); SUGA Y (SUGA-I); IINO S (IINO-I); KATAOKA K (KATA-I); TAKEKOSHI K (TAKE-I)
Inventor: IINO S; ITOH T; KATAOKA K; SUGA T; TAKEKOSHI K
Number of Countries: 030 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020021142	A1	20020221	US 2001931888	A	20010820	200236	B
EP 1182460	A2	20020227	EP 2001119644	A	20010821	200236	
JP 2002139542	A	20020517	JP 200193303	A	20010328	200237	
KR 2002015294	A	20020227	KR 200150240	A	20010821	200258	
TW 497194	A	20020801	TW 2001120363	A	20010820	200330	

Priority Applications (No Type Date): JP 200193303 A 20010328; JP 2000249702 A 20000821
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020021142	A1		22	G01R-031/26	
EP 1182460	A2	E		G01R-001/067	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002139542	A		11	G01R-031/26	
KR 2002015294	A			G01N-027/30	
TW 497194	A			H01L-021/66	

Abstract (Basic): US 20020021142 A1
Abstract (Basic):
NOVELTY - The method involves bringing two **probe electrodes** (5A,5B) into contact with oxide film (O) on semiconductor device (D) **inspection electrode** (P) and applying voltage between them so as to induce **fritting** and breakage of oxide film. One **probe** is removed from surface of device using piezo element, bimetal or electrostatic element and the other **probe** is then used to inspect electrical characteristics of device.
USE - For inspecting electrical characteristics of semiconductor devices on a wafer or packaged semiconductor devices.
ADVANTAGE - Less pressure is required to be applied to the **probe** to obtain sound electrical contact with the device. Damage done to the device **inspection electrode** is eliminated and **probe** life is prolonged. Eliminates the need to clean the **probe**, thereby improving **inspection** efficiency.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic of the apparatus used in the method.
Probe electrodes (5A,5B)
Semiconductor device (D)
Oxide film (O)
Inspection electrode (P)

pp; 22 DwgNo 1/22

49/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7714207 INSPEC Abstract Number: B2003-10-2570A-004
Title: Characterization of **fritting phenomena** on Al **electrode** for low contact force **probe** card
Author(s): Kataoka, K.; Itoh, T.; Suga, T.
Author Affiliation: Univ. of Tokyo, Japan
Journal: IEEE Transactions on Components and Packaging Technologies vol.26, no.2 p.382-7
Publisher: IEEE,
Publication Date: June 2003 Country of Publication: USA
CODEN: ITCPFB ISSN: 1521-3331
SICI: 1521-3331(200306)26:2L.382:CFPE;1-#
Material Identity Number: H324-2003-003
U.S. Copyright Clearance Center Code: 1521-3331/03/$17.00
Language: English
Abstract: We have investigated the characteristics of **fritting** of thin oxide film on an aluminum **electrode** for application to a **probe** card with low contact force. The **fritting** is a kind of electric breakdown of oxide film on metal **electrode**. It can be utilized for making electric contacts between the test **probe** and the **electrode** on LSI **chips** without a large force. The voltage and the contact force needed to cause **fritting** on a sputtered Al film was measured using W, BeCu and Pd needle **probes**. The contact resistance was also measured. A **fritting** was occurred by applying a contact load of 1 mN and voltage of 5 V. The contact resistance decreases with increasing the maximum current that passes through the contact. A current of 500 mA is enough to obtain the contact resistance of 1 Omega , which is low enough in practical test of signal lines. No damages were found on the Al film by optical microscope and scanning electron microscope observation.
Subfile: B

49/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7623041 INSPEC Abstract Number: B2003-06-2575F-030
Title: Electroplating Ni micro-cantilevers for low contact-force **IC probing**
Author(s): Kataoka, K.; Kawamura, S.; Itoh, T.; Ishikawa, K.; Honma, H.; Suga, T.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Univ. of Tokyo, Japan
Journal: Sensors and Actuators A (Physical) vol.A103, no.1-2 p. 116-21
Publisher: Elsevier,
Publication Date: 15 Jan. 2003 Country of Publication: Switzerland
CODEN: SAAPEB ISSN: 0924-4247
SICI: 0924-4247(20030115)A103:1/2L.116:EMCC;1-D
Material Identity Number: N866-2003-002
U.S. Copyright Clearance Center Code: 0924-4247/03/$30.00
Language: English
Abstract: We present a new MEMS **probe** card made of electroplated

nickel micro-cantilevers, which has compliant structures, and uses a kind of electric breakdown, or **fritting**, to make electric contacts to **electrodes** on ICs. The characteristics of **fritting** contact between nickel **probe** and Al **electrodes** were investigated, and nickel was found to have lower contact resistance than other materials. A micro-machining process for the **probe** cards, including deposition of layers having different internal stress to make a protruding cantilever shape, was developed. It was found that the **fritting** process using the micro-cantilevers could make the low-resistance contacts with the force of less than a few micronewtons.
Subfile: B

49/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

7528812 INSPEC Abstract Number: B2003-03-2570A-026
Title: Low contact force **probing** on copper **electrodes**
Author(s): Kataoka, K.; Itoh, T.; Okumura, K.; Suga, T.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Univ. of Tokyo, Japan
Conference Title: Proceedings International Test Conference 2002 (Cat. No.02CH37382) p.424-9
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xvi+1250 pp.
ISBN: 0 7803 7542 4 Material Identity Number: XX-2002-02886
U.S. Copyright Clearance Center Code: 0-7803-7542-4/02/$17.00
Conference Title: 2002 International Test Conference
Conference Sponsor: IEEE Comput. Soc. Test Technol. Tech. Council; IEEE Philadelphia Sect
Conference Date: 7-10 Oct. 2002 Conference Location: Baltimore, MD, USA
Language: English
Abstract: A contact method between **IC pads** and **probes** at low contact force is a key to developing a **probe** card with over ten thousand **probes** and MEMS **probe** cards. In this paper, we have investigated the characteristics of new low-force contact methods on Cu **electrodes** in addition to Al **electrodes**. One method is to use an electric breakdown by applying voltage to the **electrodes**, and another one is to deoxidize the native oxide on the surface of the Cu **electrode** before **probing**. A conventional needle **probe** card of tungsten **probes** was used for the experiment. At a contact force of 1 mN, a contact resistance of less than 2 Omega was obtained by the deoxidization process, and 0.7 Omega was obtained by a combination of both the oxidation and electric breakdown by applying 10 V.
Subfile: B

49/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

7364950 INSPEC Abstract Number: B2002-10-2575-018
Title: Characteristics of low force contact process for MEMS **probe** cards

Author(s): Itoh, T.; Kataoka, K.; Suga, T.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Univ. of Tokyo, Japan
Journal: Sensors and Actuators A (Physical) Conference Title: Sens. Actuators A, Phys. (Switzerland) vol.A97-98 p.462-7
Publisher: Elsevier,
Publication Date: 1 April 2002 Country of Publication: Switzerland
CODEN: SAAPEB ISSN: 0924-4247
SICI: 0924-4247(20020401)A9798L.462:CFCP;1-2
Material Identity Number: N866-2002-005
U.S. Copyright Clearance Center Code: 0924-4247/02/$22.00
Conference Title: Proceedings of 11th International Conference on Solid State Sensors and Actuators Transducers '01/Eurosensors XV
Conference Date: 10-14 June 2001 Conference Location: Munich, Germany
Language: English
Abstract: Using an atomic force microscope (AFM) system and micromachined cantilever **probes** , we have investigated the relationship between contact forces and the **fritting** which should be utilized for making contact to **IC pads** in MEMS **probe** cards. As a result, it has been clarified that a stable low-resistance contact to Al and Cu films can be obtained without applying contact forces larger than 15 mu N, when the applied voltage is larger than 15 V. Also, we have found that then the adhesion forces between the **probe** and films are less than 45 mu N. In addition, the applicability of an electroplated-Ni cantilever **probe** card to the test of 20 mu m-pitch **pad** ICs is discussed.
Subfile: B

49/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

7327952 INSPEC Abstract Number: B2002-08-2575F-088
Title: Low contact-force and compliant MEMS **probe** card utilizing **fritting** contact
Author(s): Kataoka, K.; Kawamura, S.; Itoh, T.; Suga, T.; Ishikawa, K.; Honma, H.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Univ. of Tokyo, Japan
Conference Title: Technical Digest. MEMS 2002 IEEE International Conference. Fifteenth IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.02CH37266) p.364-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xliii+737 pp.
ISBN: 0 7803 7185 2 Material Identity Number: XX-2002-00446
U.S. Copyright Clearance Center Code: 0-7803-7185-2/02/$10.00
Conference Title: Technical Digest. MEMS 2002 IEEE International Conference. Fifteenth IEEE International Conference on Micro Electro Mechanical Systems
Conference Sponsor: IEEE; Robotics & Autom. Soc
Conference Date: 20-24 Jan. 2002 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: We present a new MEMS **probe** card made of electroplated Ni micro-cantilevers, which has compliant structures, and uses a kind of electric breakdown, or **fritting**, to make electric contacts to **electrodes** on ICs. The characteristics of **fritting** contact

between Ni **probe** and Al **electrodes** were investigated, and Ni was found to have lower contact resistance than other materials. A micro-machining process for the **probe** cards, including deposition of layers having different internal stress to make a protruding cantilever shape, was developed.
Subfile: B

49/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

7084650 INSPEC Abstract Number: B2001-12-2180-001
Title: Applicability of **fritting** contacts to micromachined **probe** cards
Author(s): Itoh, T.; Kataoka, K.; Suga, T.
Journal: Journal of the Japan Society of Precision Engineering vol.67, no.8 p.1239-43
Publisher: Japan Soc. Precision Eng,
Publication Date: Aug. 2001 Country of Publication: Japan
CODEN: JJPEAD ISSN: 0912-0289
SICI: 0912-0289(200108)67:8L.1239:AFCM;1-V
Material Identity Number: J190-2001-016
Language: Japanese
Abstract: The **fritting** of thin oxide on metal surface is indispensable to realize micromachined **probe** cards, because each microprobe cannot endure the force required to break the oxide on the surface of **IC pads** mechanically. In order to clarify the force required for **fritting** -contact making, the relationship between contact forces and the **fritting** has been investigated using an atomic force microscope (AFM) system and micromachined cantilever **probes** with a pyramidal tip. The following results are obtained on the **fritting** between electroplated Au tip and Al or Cu films: (1) a stable low-resistance contact to Al and Cu films can be obtained without applying contact forces larger than 30 mu N, when the applied voltage is larger than 15 V; (2) the adhesion forces between the **probe** and films are less than 30 mu N; (3) the **fritting** contact of Cu film is easily obtained with low contact force and low applied voltage compared to that of Al film; and (4) contact resistance decreases with increasing **fritting** current. In addition, it is concluded that **probe** cards consisting of micromachined cantilevers can be applied to the test of peripheral **pad** configuration **IC** with the **pad** pitch of 20 mu m, in consequence of simple calculations.
Subfile: B

49/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6807776 INSPEC Abstract Number: B2001-02-2575F-022
Title: MEMS **IC** test **probe** utilizing **fritting** contacts
Author(s): Itoh, T.; Kataoka, K.; Engelmann, G.; Wolf, J.; Ehrmann, O.; Reichl, H.; Suga, T.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Tokyo Univ., Japan

Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4019 p.244-9
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2000 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2000)4019L.244:MTPU;1-V
Material Identity Number: C574-2000-171
U.S. Copyright Clearance Center Code: 0277-786X/2000/$15.00
Conference Title: Design, Test, Integration, and Packaging of MEMS/MOEMS
Conference Sponsor: CNRS-INPG-UJF; IEEE; IEEE Comput. Soc
Conference Date: 9-11 May 2000 Conference Location: Paris, France
Language: English
Abstract: This paper describes how a micro-electro-mechanical system (MEMS) **probe** can be applied to **IC** testing. MEMS **probe** cards are requisite to tests of higher **pad**-density and smaller **pad**-pitch **chips** with high-speed signals above 1 GHz. In addition, if a microactuator is integrated into each **probe**, we can realize a novel **probe** card in which contacts can directly be cannot generate or endure the force required to break the oxide on an Al **pad** surface mechanically. Furthermore, for the design of the switching **probe** card, the force necessary to disconnect the contact should be clarified. We experimentally switched on and off. The critical problem of the micromachined **probe** cards, however, is that each micromachined **probe** found that the **fritting** makes it possible to get low resistance contact to Al **pads** without applying external forces. Using the Au bump, the contact resistance to Al **pads** was about 0.3 Omega and the disconnection force was around 0.3 mN. In this report, we have carried out analytical calculation to estimate the performance of three different cantilever-type microactuator mechanism and to select and design the microactuator suitable for the switching **probe** card.
Subfile: B

49/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

6588413 INSPEC Abstract Number: B2000-06-2570A-052
Title: Characteristics of **fritting** contacts utilized for micromachined wafer **probe** cards
Author(s): Itoh, T.; Suga, T.; Engelmann, G.; Wolf, J.; Ehrmann, O.; Reichl, H.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Tokyo Univ., Japan
Journal: Review of Scientific Instruments vol.71, no.5 p.2224-7
Publisher: AIP,
Publication Date: May 2000 Country of Publication: USA
CODEN: RSINAK ISSN: 0034-6748
SICI: 0034-6748(200005)71:5L.2224:CFCU;1-C
Material Identity Number: R017-2000-005
U.S. Copyright Clearance Center Code: 0034-6748/2000/71(5)/2224(4)/$17.00
Language: English
Abstract: We have investigated the relationship between contact forces and the **fritting** which should be utilized for making contact to **integrated circuit pads** in micromachined wafer **probe** cards. Micromachined **probe** cards are requisite to tests

of higher **pad**-density and smaller **pad**-pitch **chips** with high-speed signals above 1 GHz. In addition, if a microactuator is integrated into each **probe**, we can realize a novel **probe** card in which contacts can directly be switched on and off. The critical problem of the micromachined **probe** cards, however, is that each micromachined **probe** cannot generate or endure the force required to break the oxide on an Al **pad** surface mechanically. To overcome the problem, we planned to reduce the required contact force by putting the **fritting** effect to good use. For that, in this article, we have measured forces required for making contact to Al **pads** and contact resistance when utilizing the **fritting** process for the break of the **pad** surface oxide. Furthermore, we have also measured the force necessary to disconnect the contact made by the **fritting**, since it is important to design the **probe** dimensions and integrated actuators. As a result, we have found that the **fritting** makes it possible to get low resistance contact to Al **pads** without applying external forces. Moreover, the contact resistance and the adhesion force, when using electroplated Au bumps as the contact **probe** , were found to be one-third of those when using electroplated Ni bumps, respectively. This indicates that the Au bump is more suitable for the **probe** of micromachined **probe** cards.
Subfile: B

49/3,AB/9 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05561705
E.I. No: EIP00055175457
Title: Applicability of MEMS **probe** card to wafer-level test
Author: Itoh, Toshihiro; Suga, Tadatomo; Engelmann, Gunter; Wolf, Juergen ; Ehrmann, Oswin; Reichl, Herbert
Corporate Source: Univ of Tokyo, Tokyo, Jpn
Conference Title: InterPACK '99: Pacific RIM/ASME International Intersociety Electronics Photonic Packaging Conference 'Advances in Electronic Packaging 1999'
Conference Location: Maui, HI, USA Conference Date: 19990613-19990619
Source: American Society of Mechanical Engineers, EEP v 26 (1) 1999. ASME, USA. p 123-130
Publication Year: 1999
CODEN: EEAEEM
Language: English
Abstract: In the following, it shall be described how an active **probe** card can be applied to full electrical wafer-level testing, using a micro-electro-mechanical system (MEMS). Although various technologies have been proposed for making contact to all **pads** on a wafer simultaneously, methods to connect the huge numbers of signal terminals to the outside testers have hardly been investigated. In order to reduce the necessary terminals, we propose a new type of **probe** card in which each **probe** have an integrated microactuator and a group of these **probes** is connected to a single wiring line. In testing, only one **probe** of the group is actuated and brought into contact to the corresponding **pad**. In this way, all **pads** of the dies that are tested simultaneously get into contact with their respective **probe**. The problem of the microfabricated active **probe** is, however, that it can produce only a low force of approximately 1 mN, which is much smaller than the forces required for conventional scrubbing **probes**. The

reason for it is that its dimensions should be in the range of the **pad** pitches and compliance is required to compensate the **probe-pad** distance deviation of at least several micrometers. To get a low resistance at small contact forces, we propose a special **probe** configuration that will allow the **fritting** process on **IC pads**. Finally, calculations were carried out to estimate the performance of three different microactuation mechanisms and to select and design the microactuator suitable for the new type of **probe** card. (Author abstract) 12 Refs.

49/3,AB/10 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

04408888 INSIDE CONFERENCE ITEM ID: CN046156493
Development of MEMS **IC Probe** Card Utilizing **Fritting** Contact
Itoh, T.; Kataoka, K.; Suga, T.
CONFERENCE: International conference on precision engineering; Initiatives of precision engineering at the beginning of a millennium (ICPE)-10th
P: 314-318
Boston, London, Kluwer Academic Publishers, c2001
ISBN: 0792374142
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE EDITOR(S): Inasaki, I.
CONFERENCE LOCATION: Yokohama, Japan 2001; Jul (200107) (200107)

29sep03 10:55:15 User267149 Session D1030.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2003/Sep W3
(c) 2003 Institution of Electrical Engineers
*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2003/Sep W4
(c) 2003 NTIS, Intl Cpyrght All Rights Res
File 8:Ei Compendex(R) 1970-2003/Sep W3
(c) 2003 Elsevier Eng. Info. Inc.
File 34:SciSearch(R) Cited Ref Sci 1990-2003/Sep W3
(c) 2003 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2003/Aug
(c) 2003 ProQuest Info&Learning
File 65:Inside Conferences 1993-2003/Sep W4
(c) 2003 BLDSC all rts. reserv.
File 94:JICST-EPlus 1985-2003/Sep W3
(c)2003 Japan Science and Tech Corp(JST)
File 99:Wilson Appl. Sci & Tech Abs 1983-2003/Aug
(c) 2003 The HW Wilson Co.
File 144:Pascal 1973-2003/Sep W3
(c) 2003 INIST/CNRS
File 305:Analytical Abstracts 1980-2003/Sep W1
(c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2003/Aug
(c) 2003 DECHEMA
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200361
(c) 2003 Thomson Derwent
File 347:JAPIO Oct 1976-2003/May(Updated 030902)
(c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2003/Apr
(c) 2003 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	2058	AU=(IINO, S? OR IINO S?)
S2	230	AU=(TAKEKOSHI, K? OR TAKEKOSHI K?)
S3	0	AU=(SUGA, T? OT SUGA T?)
S4	0	AU=(ITOH, T? OT ITOH T?)
S5	8071	AU=(KATAOKA, K? OR KATAOKA K?)
S6	7	S1 AND S2
S7	7	RD (unique items)
S8	2	S7 AND S5
S9	5	S7 NOT S8
S10	5	RD (unique items)
S11	2	S1 AND S5
S12	0	S11 NOT S6
S13	2	S2 AND S5
S14	0	S13 NOT S11
S15	10350	S1,S2,S5
S16	27	S15 AND (INSPECT???????? OR ANALYZ??????? OR ANALYS??????)-(3N)(PROBE???? OR PROBING OR (INTEGRAT????????(3N)(CIRCUIT???-?????? OR LOOP? ?) OR IC OR CHIP? ? OR ELECTRODE? ? OR PAD? ?))
S17	23	S16 NOT S7
S18	1	S17 AND FRITTING
S19	22	S17 NOT S18
S20	13	S19 AND (PROBE???? OR PROBING)
S21	13	RD (unique items)
S22	9	S19 NOT S20
S23	8	RD (unique items)

8/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014507939
WPI Acc No: 2002-328642/200236
XRPX Acc No: N02-257899
Semiconductor device inspection method for measuring electrical characteristics, involves applying a voltage between two probes in contact with oxide film to induce fritting and breakage of film
Patent Assignee: ITOH T (ITOH-I); SUGA T (SUGA-I); TOKYO ELECTRON LTD (TKEL); ITO K (ITOK-I); SUGA Y (SUGA-I); IINO S (IINO-I); KATAOKA K (KATA-I); TAKEKOSHI K (TAKE-I)
Inventor: **IINO S**; ITOH T; **KATAOKA K**; SUGA T; **TAKEKOSHI K**
Number of Countries: 030 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020021142	A1	20020221	US 2001931888	A	20010820	200236	B
EP 1182460	A2	20020227	EP 2001119644	A	20010821	200236	
JP 2002139542	A	20020517	JP 200193303	A	20010328	200237	
KR 2002015294	A	20020227	KR 200150240	A	20010821	200258	
TW 497194	A	20020801	TW 2001120363	A	20010820	200330	

Priority Applications (No Type Date): JP 200193303 A 20010328; JP 2000249702 A 20000821
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020021142	A1		22	G01R-031/26	
EP 1182460	A2	E		G01R-001/067	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002139542	A		11	G01R-031/26	
KR 2002015294	A			G01N-027/30	
TW 497194	A			H01L-021/66	

Abstract (Basic): US 20020021142 A1
Abstract (Basic):

NOVELTY - The method involves bringing two probe electrodes (5A,5B) into contact with oxide film (O) on semiconductor device (D) inspection electrode (P) and applying voltage between them so as to induce fritting and breakage of oxide film. One probe is removed from surface of device using piezo element, bimetal or electrostatic element and the other probe is then used to inspect electrical characteristics of device.

USE - For inspecting electrical characteristics of semiconductor devices on a wafer or packaged semiconductor devices.

ADVANTAGE - Less pressure is required to be applied to the probe to obtain sound electrical contact with the device. Damage done to the device inspection electrode is eliminated and probe life is prolonged. Eliminates the need to clean the probe, thereby improving inspection efficiency.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic of the apparatus used in the method.

Probe electrodes (5A,5B)
Semiconductor device (D)
Oxide film (O)
Inspection electrode (P)

pp; 22 DwgNo 1/22

8/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07271079
INSPECTION METHOD AND INSPECTION DEVICE

PUB. NO.: 2002-139542 [JP 2002139542 A]
PUBLISHED: May 17, 2002 (20020517)
INVENTOR(s): **IINO SHINJI**
TAKEKOSHI KIYOSHI
SUGA TADATOMO
ITO HISAHIRO
KATAOKA KENICHI
APPLICANT(s): TOKYO ELECTRON LTD
SUGA TADATOMO
ITO HISAHIRO
APPL. NO.: 2001-093303 [JP 20011093303]
FILED: March 28, 2001 (20010328)
PRIORITY: 2000-249702 [JP 2000249702], JP (Japan), August 21, 2000 (20000821)

ABSTRACT

PROBLEM TO BE SOLVED: To solve such problems in an inspection method that the service life of a probe N is shortened by scrubbing and that yield of a device is reduced by damaging the inspection electrode P as shown in (b) of figure 7 when the probe N is brought into contact with an inspection electrode P electrically by scrubbing operation.

SOLUTION: This inspection method for executing electric characteristic inspection of the device by bringing an inspection probe 12A into electric contact with the inspection electrode P, has a contact process for bringing the inspection probe 12A into electric contact with the inspection electrode P by breaking an insulating coat O of the inspection electrode P by utilizing fritting phenomenon.

10/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013531266
WPI Acc No: 2001-015472/200102
XRPX Acc No: N01-011756
Contactor holding mechanism and automatic change mechanism for contactor
Patent Assignee: TOKYO ELECTRON LTD (TKEL)
Inventor: HAGIHARA J; **IINO S**; **TAKEKOSHI K**
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200045433	A1	20000803	WO 2000JP442	A	20000128	200102	B
JP 2000286313	A	20001013	JP 99296484	A	19991019	200102	
KR 2001024959	A	20010326	KR 2000710643	A	20000926	200161	

US 6590381 B1 20030708 WO 2000JP442 A 20000128 200353
US 2000646951 A 20000925

Priority Applications (No Type Date): JP 99296484 A 19991019; JP 9922985 A 19990129

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200045433	A1	J		H01L-021/66	
Designated States (National): KR US					
JP 2000286313	A		10	H01L-021/66	
KR 2001024959	A			H01L-021/66	
US 6590381	B1			G01R-031/02	Based on patent WO 200045433

Abstract (Basic): WO 200045433 A1

Abstract (Basic):

NOVELTY - A contactor holding mechanism and an automatic contactor change mechanism having the contactor holding mechanism; the contactor holding mechanism comprising a frame body (11) fixed to a performance board (P), a plurality of latch mechanisms (13) for holding a contactor inside the frame body, and a fixedly sucking mechanism (14) for fixing the contactor held by the latch mechanisms inside the frame body usign a vacuum sucking force; the automatic contactor change mechanism comprising a holding mechanism (10) detachably holding the contactor and a transfer mechanism (16) transferring the contactor (12) between it and the holding mechanism, the transfer mechanism comprising a sucking and holding part (17) sucking and holding the contactor (12) between it and the holding mechanism, the transfer mechanism comprising a sucking and holding part (17) sucking and holding the contactor (12), a swingable and liftable arm (18) having the sucking and holding part at the tip of the arm, and an arm drive part (19) to swing and lift the arm (18).

USE - None given.

pp; 0 DwgNo 0/0

10/3,AB/2 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010777883

WPI Acc No: 1996-274836/199628

Related WPI Acc No: 1996-249116

XRPX Acc No: N96-231222

Inspection device e.g for semiconductor wafer in TFT, LCD substrate mfr - has positioning control unit that performs positioning control of inspection target, based on position information output by mark image transmission part

Patent Assignee: TEL ENG KK (TKEL); TOKYO ELECTRON LTD (TKEL); TEL ENG LTD (TELE-N)

Inventor: IIDA I; **IINO S**; **TAKEKOSHI K**

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8115954	A	19960507	JP 94249483	A	19941014	199628	B
TW 273011	A	19960321	TW 95108256	A	19950808	199628	
US 5691764	A	19971125	US 95510669	A	19950803	199802	
KR 272190	B	20001201	KR 9524237	A	19950805	200173	

Priority Applications (No Type Date): JP 94249483 A 19941014; JP 94184375 A 19940805
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8115954	A		12	H01L-021/66	
TW 273011	A			G01R-031/02	
US 5691764	A		27	H04N-007/18	
KR 272190	B			H01L-021/66	Previous Publ. patent KR 96009091

Abstract (Basic): JP 8115954 A

The inspection device has a probe board (25) consisting of probe electrode (33) which performs electric inspection of an inspection target (2). The inspection position of the inspection target at which a number of electrode contact points (30) are provided, contacts the inspection target through an electrode contact point.

A pair of crossing marks (31a,31b) are used to align the inspection target to the inspection position. A conveyance part (5) conveys the inspection target among the alignment positions other than the inspection position. On a stage (3), a CCD camera (34) is provided for image pick-up. A positioning control unit performs the positioning control of the inspection target, based on the position information from an alignment block (35). The alignment block leads the image to the CCD camera.

ADVANTAGE - Enables usage of one set of image pick up unit for alignment. Performs direct check of contact parts. Minimizes inspection time of target. Performs alignment of inspection target efficiently.

Dwg.1/11

Abstract (Equivalent): US 5691764 A

The inspection device has a probe board (25) consisting of probe electrode (33) which performs electric inspection of an inspection target (2). The inspection position of the inspection target at which a number of electrode contact points (30) are provided, contacts the inspection target through an electrode contact point.

A pair of crossing marks (31a,31b) are used to align the inspection target to the inspection position. A conveyance part (5) conveys the inspection target among the alignment positions other than the inspection position. On a stage (3), a CCD camera (34) is provided for image pick-up. A positioning control unit performs the positioning control of the inspection target, based on the position information from an alignment block (35). The alignment block leads the image to the CCD camera.

ADVANTAGE - Enables usage of one set of image pick up unit for alignment. Performs direct check of contact parts. Minimizes inspection time of target. Performs alignment of inspection target efficiently.

Dwg.1/21b

10/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010752161
WPI Acc No: 1996-249116/199625
Related WPI Acc No: 1996-274836
XRPX Acc No: N96-209369

Semiconductor wafer e.g. LCD substrate inspection device - has controller to control movable part to inspect substrates on two stands

Patent Assignee: TEL ENG KK (TKEL); TOKYO ELECTRON LTD (TKEL); TEL ENG

LTD (TELE-N)
Inventor: IIDA I; **IINO S**; **TAKEKOSHI K**
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8102476	A	19960416	JP 95182449	A	19950719	199625	B
TW 273011	A	19960321	TW 95108256	A	19950808	199628	
US 5691764	A	19971125	US 95510669	A	19950803	199802	
KR 272190	B	20001201	KR 9524237	A	19950805	200173	

Priority Applications (No Type Date): JP 94184375 A 19940805; JP 94249483 A 19941014
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8102476	A		14	H01L-021/66	
TW 273011	A			G01R-031/02	
US 5691764	A		27	H04N-007/18	
KR 272190	B			H01L-021/66	Previous Publ. patent KR 96009091

Abstract (Basic): JP 8102476 A

The inspection device consists of a probe device (1) which comprises an LCD substrate accommodation part (2). A processor (3) is also provided. A conveyance part (4) is present between the accommodation part and the processor. An inspection mechanism (20) with a probe card (43) is positioned in the inspection domain (21) of the processor. Two right and left alignment domains (22a,22b) are provided across facing the inspection domain.

Two positioning stands (31a,31b) are positioned separately on the inspection domain. The LCD substrate (ST) to be inspected is placed on the positioning stands. The stands are moved between the two alignment domains by a movable part. A controller (51) controls the movable part. Thus the LCD substrates on both the stands are inspected in turns in the inspection domain.

ADVANTAGE - Reduces time of inspection.

Dwg.1/10

Abstract (Equivalent): US 5691764 A

The inspection device has a probe board (25) consisting of probe electrode (33) which performs electric inspection of an inspection target (2). The inspection position of the inspection target at which a number of electrode contact points (30) are provided, contacts the inspection target through an electrode contact point.

A pair of crossing marks (31a,31b) are used to align the inspection target to the inspection position. A conveyance part (5) conveys the inspection target among the alignment positions other than the inspection position. On a stage (3), a CCD camera (34) is provided for image pick-up. A positioning control unit performs the positioning control of the inspection target, based on the position information from an alignment block (35). The alignment block leads the image to the CCD camera.

ADVANTAGE - Enables usage of one set of image pick up unit for alignment. Performs direct check of contact parts. Minimizes inspection time of target. Performs alignment of inspection target efficiently.

Dwg.1/21b

10/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06700482
HOLDING MECHANISM AND AUTOMATIC REPLACEMENT MECHANISM FOR CONTACTOR

PUB. NO.: 2000-286313 [JP 2000286313 A]
PUBLISHED: October 13, 2000 (20001013)
INVENTOR(s): **IINO SHINJI**
HAGIWARA JUNICHI
TAKEKOSHI KIYOSHI
APPLICANT(s): TOKYO ELECTRON LTD
APPL. NO.: 11-296484 [JP 99296484]
FILED: October 19, 1999 (19991019)
PRIORITY: 11-022985 [JP 9922985], JP (Japan), January 29, 1999 (19990129)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a holding mechanism for a contactor wherein a contactor itself where multiple probes of, for example bump type are formed, is held detachably for enhanced inspection accuracy, and to provide an automatic replacement mechanism for contactor wherein a contactor is automatically replaced for the contactor holding mechanism for enhanced inspection throughput.

SOLUTION: This automatic replacement mechanism 20 comprises a holding mechanism 10 which detachably holds a contactor, and a delivery mechanism 16 for delivery between the holding mechanism 10 and a contactor 12. The delivery mechanism 16 comprises a sucking/holding part 17 which sucks and holds the contactor 12, an arm 18 which comprises the sucking/holding part 17 at its tip part while rotation and rising/falling allowed, and an arm drive part which rotates or elevates/descends the arm 18.

10/3,AB/5 (Item 2 from file: 347)

05160454
INSPECTION EQUIPMENT

PUB. NO.: 08-115954 [JP 8115954 A]
PUBLISHED: May 07, 1996 (19960507)
INVENTOR(s): **IINO SHINJI**
TAKEKOSHI KIYOSHI
IIDA ITARU
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
TERU ENG KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-249483 [JP 94249483]
FILED: October 14, 1994 (19941014)

ABSTRACT

PURPOSE: To shorten the inspection time by widening the work space above the inspecting position of an inspection equipment thereby performing the alignment of an object efficiently while allowing direct recognition of the

contact means in the inspection means using a single image pickup means for alignment.

CONSTITUTION: Under a state where a CCD camera 34 for picking up the image of the probe electrode in a probe board 25 and a stage 3 are transferred to an alignment position on the stage 3 side of an object 2, an alignment block 35 is provided in order to introduce the images of two alignment marks 31a, 31b of the object 2 to the CCD camera 34. Position of the object 2 is then adjusted based on the positional information of the images of the marks 31a, 31b.

18/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06282462
E.I. No: EIP03047340255
Title: Electroplating Ni micro-cantilevers for low contact-force IC probing
Author: **Kataoka, Kenichi**; Kawamura, Shingo; Itoh, Toshihiro; Ishikawa, Kaoru; Honma, Hideo; Suga, Tadatomo
Corporate Source: Res. Ctr. for Adv. Sci. and Technol. University of Tokyo, Tokyo 153-8904, Japan
Source: Sensors and Actuators, A: Physical v 103 n 1-2 Jan 15 2003. p 116-121
Publication Year: 2003
CODEN: SAAPEB ISSN: 0924-4247
Language: English
Abstract: We present a new MEMS probe card made of electroplated nickel micro-cantilevers, which has compliant structures, and uses a kind of electric breakdown, or **fritting**, to make electric contacts to electrodes on ICs. The characteristics of **fritting** contact between nickel probe and Al electrodes were investigated, and nickel was found to have lower contact resistance than other materials. A micro-machining process for the probe cards, including deposition of layers having different internal stress to make a protruding cantilever shape, was developed. It was found that the **fritting** process using the micro-cantilevers could make the low-resistance contacts with the force of less than a few micronewtons. copy 2003 Elsevier Science B.V. All rights reserved. 10 Refs.

21/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02639690 Genuine Article#: LT368 Number of References: 40
Title: 2 NEW MEMBERS OF THE MAF ONCOGENE FAMILY, MAFK AND MAFF, ENCODE NUCLEAR B-ZIP PROTEINS LACKING PUTATIVE TRANSACTIVATOR DOMAIN (Abstract Available)
Author(s): FUJIWARA KT; **KATAOKA K**; NISHIZAWA M
Corporate Source: JAPANESE FDN CANC RES,INST CANC,DEPT VIRAL ONCOL,1-37-1 KAMI IKEBUKURO,TOSHIMA KU/TOKYO 170//JAPAN/; JAPANESE FDN CANC RES,INST CANC,DEPT VIRAL ONCOL,1-37-1 KAMI IKEBUKURO,TOSHIMA KU/TOKYO 170//JAPAN/
Journal: ONCOGENE, 1993, V8, N9 (SEP), P2371-2380
ISSN: 0950-9232
Language: ENGLISH Document Type: ARTICLE
Abstract: The v-maf oncogene of the avian musculoaponeurotic fibrosarcoma virus, AS42, encodes a nuclear protein which contains a characteristic b-Zip domain. By screening a chicken embryo fibroblast (CEF) cDNA library under moderately stringent hybridization conditions, we picked up a series of cDNA clones for a novel maf-related gene which we named mafK. We also identified another maf-related gene named mafF by screening a chicken genomic library using a mafK **probe**. Structural **analyses** suggested that the mafK and mafF genes consist of three exons. The exon-intron structures of the two genes resemble each other, but differ from that of the chicken c-maf gene. As compared to the c-Maf protein, the proteins encoded by the mafK and the mafF genes are rather small in size and lack the regions corresponding to the amino terminal acidic domain present in the c-Maf protein. On the other hand, the structures of the b-Zip domain are well conserved among these Maf-related proteins. When overexpressed by using an avian retroviral vector, the two maf-related genes did not induce morphological transformation of CEF cells but induced colony formation in soft agar with very low efficiencies. With a specific antibody, the MafK protein was detected predominantly in the nuclei of the cells infected with the virus which carries the mafK gene. Tissue distributions of these three maf-family genes are different from one another, probably reflecting their different functions in vivo.

21/3,AB/2 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03142668 JICST ACCESSION NUMBER: 97A0426195 FILE SEGMENT: JICST-E
Effects of Temperature Stress on Adhesive Abilities and Antigenicity of Porphyromonas gingivalis.
AMANO ATSUO (1); KUBONIWA MASAE (1); HORIE HIROSHI (1); **KATAOKA KOSUKE** (1); NAGATA HIDEKI (1); SHIZUKUISHI SATOSHI (1)
(1) Osaka Univ., Fac. of Dent.
Nippon Shishubyo Gakkai Kaishi(Journal of the Japanese Association of Periodontalogy), 1997, VOL.39,NO.1, PAGE.86-92, FIG.4, REF.20
JOURNAL NUMBER: S0411CAY ISSN NO: 0385-0110
UNIVERSAL DECIMAL CLASSIFICATION: 579.22:616-022.1 616.31-09
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication
ABSTRACT: Periodontopathic bacteria are able to survive various changes of their environment due to the undergoing advances of periodontal diseases. There are mechanisms which regulate the alternation of bacterial metabolism and protein expression to adapt physiological functions to environmental stresses due to changes of temperature, pH ratio and nutrients. In this study, we examined the effect of a 2.DEG.C. elevation of temperature on adhesive abilities and antigenicity of Porphyromonas gingivalis. P. gingivalis ATCC 33277 was grown at 37.DEG.C. to the stationary phase. Inoculums(1%) from the culture were further incubated at 37.DEG.C., and 39.DEG.C. to investigate stress due to elevation in temperature in the stationary phase. There was no difference in the growth curves of cells at 37.DEG.C. and 39.DEG.C.. However, observations of cell surfaces by an electron microscope revealed that cells grown at 39.DEG.C. expressed little filamentous structure of fimbriae which can be observed in 37.DEG.C.-cells. 39.DEG.C.-cells significantly lost binding abilities to hydroxyapatite beads(HAP) coated with whole saliva and their specific salivary receptors, proline-rich protein and statherin. Coaggregation activity of 39.DEG.C.-cells with Streptococcus oralis was reduced by 92% of that of 37.DEG.C.-cells. Whole cells at 37 and 39.DEG.C. were loaded to SDS-PAGE for western blot **analysis** and were **probed** with marginal periodontitis-patient serum. Major reaction bands of 37.DEG.C.-cells were detected at 75, 43, 40, 34, and 29 kDa positions. In the profile of **probed** bands of 39.DEG.C.-cells, densities of these major bands were significantly reduced, and several new bands were observed with a wide range of molecular sizes. These observations suggested that P.gingivalis may undergo alterations in its physiological functions and antigenicity as a result of a change of temperature which can be found with advances of several types of periodontal diseases. (author abst.)

21/3,AB/3 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00505406 JICST ACCESSION NUMBER: 87A0538784 FILE SEGMENT: JICST-E
Effects of fluoride varnish on human enamel-in vitro.
KANI MIZUO (1); KANI TOKUKO (1); **IINO SHINTARO** (1); ISOZAKI ATSUNORI (1); HIROSE AKIKO (1); KAJITA HIDEYUKI (1); KATO HIROHISA (1)
(1) Asahidai Shi
Koku Eisei Gakkai Zasshi(Journal of Dental Health), 1987, VOL.37,NO.3, PAGE.342-351, FIG.6, TBL.5, REF.20
JOURNAL NUMBER: Z0659AAP ISSN NO: 0023-2831
UNIVERSAL DECIMAL CLASSIFICATION: 615.2+ 591.131.3.05+591.431/.432 616.314:613/614
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Fluoride varnish(F-varnish) has been already used for treatment of hypersensitive dentin in clinic. In this study, F-varnish was examined in vitro the possibility of application for caries inhibition. Experiments were made in vitro of applications of F-varnish, containing 5% NaF or placebo-varnish with the intact enamel surface and fissure, for two weeks at 37.DEG.C twice a week, followed by 1, 2 or 3 weeks of washing with distilled water. Fluoride uptake and release,

morphological observation, and acid solubility test on enamel blocks following treatment with F-varnish, or after washing were studied by means of electron **probe** microanalysis(EPMA), chemical **analysis** and sacanning electron microscopy(SEM). The fluoride uptake of F-varnish-treated enamel surface and fissure were increased, especially a large amount of CaF2 deposited on the outer surface layer and fissure of enamel. Although, CaF2 was released after washing for three weeks, fluoride was taken up at the depth of approximately 40.MU.m. The acid solubility test proved that the acquisition of acid resistance was greater in F-varnish-treated enamel than in the control even after washing for three weeks. SEM of enamel surface showed that CaF2 was formed in the F-varnish-treated enamel, and clearly showed that there was an acid-resistant picture after perchloric acid-etching. Therefore, we suggest that F-varnish which applied to treat hypersensitive dentin may be effective in clinical use for caries inhibition, because the treatment time of enamel can be extended.(author abst.)

21/3,AB/4 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15307807 PASCAL No.: 01-0481926

An extremely large magnitude eruption close to the Plio-Pleistocene boundary : reconstruction of eruptive style and history of the Ebisutoge-Fukuda tephra, central Japan

KATAOKA K; NAGAHASHI Y; YOSHIKAWA S

Department of Geosciences, Osaka City University, Sugimoto 3-3-138, Sumiyoshi-ku, Osaka 558-8585, Japan; Faculty of Education, Fukushima University, Kanayagawa 1, Fukushima 960-1296, Japan

Journal: Journal of volcanology and geothermal research, 2001, 107 (1-3) 47-69

Language: English

An extremely large magnitude eruption of the Ebisutoge-Fukuda tephra, close to the Plio-Pleistocene boundary, central Japan, spread volcanic materials widely more than 290,000 km SUP 2 reaching more than 300 km from the probable source. Characteristics of the distal air-fall ash (> 150 km away from the vent) and proximal pyroclastic deposits are clarified to constrain the eruptive style, history, and magnitude of the Ebisutoge-Fukuda eruption. Eruptive history had five phases. Phase I is phreatoplinian eruption producing > 105 km SUP 3 of volcanic materials. Phases 2 and 3 are plinian eruption and transition to pyroclastic flow. Plinian activity also occurred in phase 4, which ejected conspicuous obsidian fragments to the distal locations. In phase 5, collapse of eruption column triggered by phase 4, generated large pyroclastic flow in all directions and resulted in more than 250-350 km SUP 3 of deposits. Thus, the total volume of this tephra amounts over 380-490 km SUP 3 . This indicates that the Volcanic Explosivity Index (VEI) of the Ebisutoge-Fukuda tephra is greater than 7. The huge thickness of reworked volcaniclastic deposits overlying the fall units also attests to the tremendous volume of eruptive materials of this tephra. Numerous ancient tephra layers with large volume have been reported worldwide, but sources and eruptive history are often unknown and difficult to determine. Comparison of distal air-fall ashes with proximal pyroclastic deposits revealed eruption style, history and magnitude of the Ebisutoge-Fukuda tephra. Hence, recognition of the Ebisutoge-Fukuda tephra, is useful for understanding the volcanic activity during the Pliocene to Pleistocene, is important as a boundary marker bed,

and can be used to interpret the global environmental and climatic impact of large magnitude eruptions in the past.

21/3,AB/5 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

11136303 PASCAL No.: 93-0644361
Two new members of the maf oncogene family, mafK and mafK, encode nuclear b-Zip proteins lacking putative trans-activator domain
FUJIWARA K T; **KATAOKA K**; NISHIZAWA M
Cancer inst., dep. viral oncology, Toshima-ku, Tokyo 170, Japan
Journal: Oncogene : (Basingstoke), 1993, 8 (9) 2371-2380
Language: English
The v-maf oncogene of the avian musculoaponeurotic fibrosarcoma virus, AS42, encodes a nuclear protein which contains a characteristic b-Zip domain. By screening a chicken embryo fibroblast (CEF) cDNA library under moderately stringent hybridization conditions, we picked up a series of cDNA clones for a novel maf-related gene which we named mafK. We also identified another maf-related gene named mafF by screening a chicken genomic library using a mafK **probe**. Structural **analyses** suggested that the mafK and mafF genes consist of three exons. The exon-intron structures of the two genes resemble each other, but differ from that of the chicken c-maf gene

21/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014044769
WPI Acc No: 2001-528982/200158
XRPX Acc No: N01-392589
Probe arrangement assembly for integrated **chip inspection**, has supporting plate with corresponding sections separable from conductive foil fixed to contact terminal corresponding section
Patent Assignee: TOKYO ELECTRON LTD (TKEL); HOSAKA H (HOSA-I); TAKEKOSHI K (TAKE-I)
Inventor: HOSAKA H; **TAKEKOSHI K**
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010009376	A1	20010726	US 2001765423	A	20010122	200158	B
JP 2001281268	A	20011010	JP 2000307609	A	20001006	200175	
KR 2001076394	A	20010811	KR 20013204	A	20010119	200212	
TW 476125	A	20020211	TW 2001101566	A	20010120	200304	

Priority Applications (No Type Date): JP 2000307609 A 20001006; JP 200013741 A 20000124
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010009376	A1		21	G01R-031/02	
JP 2001281268	A		13	G01R-001/073	
KR 2001076394	A			H01L-021/66	

TW 476125 A H01L-021/66

Abstract (Basic): US 20010009376 A1
Abstract (Basic):
NOVELTY - Each **probe** (4) has contact terminal (4A) fixed to free end of a supporting plate (4B). Supporting plate-corresponding sections are integrally formed with a conductive foil. Each supporting plate-corresponding section is separable from the foil. A contact terminal corresponding section is respectively fixed to one end of each of the supporting plate-corresponding sections.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) **Probe** arrangement assembly manufacturing method; and
(b) **Probe** mounting apparatus.
USE - For forming **probes** used in electrical characteristics **inspection** of **integrated circuit** (**IC**) chip.
ADVANTAGE - Several IC **chips** can be simultaneously **inspected** by using the contactor having **probes** which are manufactured at low cost without requiring exclusive photomask.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the contactor having **probes**.
Probe (4)
Contact terminal (4A)
Supporting plate (4B)
pp; 21 DwgNo 1/15

21/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013052564
WPI Acc No: 2000-224419/200019
XRPX Acc No: N00-168147
Contactor for performing electrical inspection on sample to be **inspected** by connecting **probe** terminals to electrode pads of sample to be inspected
Patent Assignee: TOKYO ELECTRON LTD (TKEL)
Inventor: HAGIHARA J; **IINO S**
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200010016	A1	20000224	WO 99JP4090	A	19990729	200019	B
JP 2000055936	A	20000225	JP 98241036	A	19980812	200021	
JP 2000121673	A	20000428	JP 99126173	A	19990506	200032	
TW 418479	A	20010111	TW 99113123	A	19990731	200132	
US 6344752	B1	20020205	WO 99JP4090	A	19990729	200211	
			US 2000509546	A	20000412		

Priority Applications (No Type Date): JP 98241037 A 19980812; JP 98241036 A 19980812
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200010016	A1	J	47	G01R-001/073	
Designated States (National): KR US					
JP 2000055936	A		8	G01R-001/073	
JP 2000121673	A		11	G01R-001/073	
TW 418479	A			H01L-021/66	

US 6344752 B1 G01R-031/02 Based on patent WO 200010016

Abstract (Basic): WO 200010016 A1
Abstract (Basic):
NOVELTY - Contactor has electrodes (3) arranged on silicon (first) substrate (2), and **probe** terminals (4) provided on the electrodes. Each **probe** terminal has conductive support (7) on the first electrode, elastic support plate (8) fixed at one end to the upper end of the conductive support, and a (bump) **probe** terminal (9) fixed to the free end of the elastic support plate.
USE - For electrical inspection on sample to be inspected.
ADVANTAGE - Easy and simple to change **probe** terminals, and has simple support structure.
DESCRIPTION OF DRAWING(S) - Drawing shows schematic structure of contactor according to the invention.
Silicon substrate (2)
Electrodes (3)
Probe terminals (4)
Conductive support (7)
Elastic support plate (8)
Probe terminal (9)
pp; 47 DwgNo 7/12

21/3,AB/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012069950
WPI Acc No: 1998-486861/199842
XRPX Acc No: N98-380405
Probe apparatus used for **IC chip inspection** - has main chuck which receives unused polish boards from accommodation mechanism into polishing area, which is then conveyed back to accommodation mechanism after polishing process
Patent Assignee: TOKYO ELECTRON LTD (TKEL)
Inventor: **TAKEKOSHI K**
Number of Countries: 028 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10209232	A	19980807	JP 9723133	A	19970122	199842	B
EP 905502	A2	19990331	EP 98101004	A	19980121	199917	
KR 98070664	A	19981026	KR 981716	A	19980121	199953	
US 6024629	A	20000215	US 9810116	A	19980121	200016	
JP 3144672	B2	20010312	JP 9723133	A	19970122	200116	
TW 405198	A	20000911	TW 98100799	A	19980121	200129	
KR 330844	B	20020620	KR 981716	A	19980121	200280	
EP 905502	B1	20030402	EP 98101004	A	19980121	200325	
DE 69812822	E	20030508	DE 612822	A	19980121	200338	
			EP 98101004	A	19980121		

Priority Applications (No Type Date): JP 9723133 A 19970122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10209232	A		11	H01L-021/66	
EP 905502	A2	E		G01N-001/32	

Designated States (Regional): AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

KR 98070664	A		H01L-021/304	
US 6024629	A		B24B-001/04	
JP 3144672	B2	11	H01L-021/66	Previous Publ. patent JP 10209232
TW 405198	A		H01L-021/66	
KR 330844	B		H01L-021/304	Previous Publ. patent KR 98070664
EP 905502	B1 E		G01R-031/28	
Designated States (Regional): DE FR GB IT				
DE 69812822	E		G01R-031/28	Based on patent EP 905502

Abstract (Basic): JP 10209232 A

The apparatus (10) includes an automatic exchange unit (30) which performs automatic exchange of a polish board (31) in a transverse plane of a **prober** (13). An accommodation mechanism (32) contains polish boards (31,31A).

One unused polish board is received from the accommodation mechanism and is conveyed to polishing area (16A) of a main chuck (16). The polish board is then received from the polishing area of chuck and is conveyed to the accommodation mechanism.

ADVANTAGE - Exchanges polish board efficiently in short time. Performs reliable **inspection** of **IC chip**.

Dwg.1/7

21/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06828851
PROBING CARD AND ITS MANUFACTURE

PUB. NO.: 2001-056345 [JP 2001056345 A]
PUBLISHED: February 27, 2001 (20010227)
INVENTOR(s): **TAKEKOSHI KIYOSHI**
APPLICANT(s): TOKYO ELECTRON LTD
APPL. NO.: 11-232779 [JP 99232779]
FILED: August 19, 1999 (19990819)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a **probing** card capable of performing highly reliable **inspections** by bringing all **probes** in reliable contact with corresponding electrode pads even if the electrode pads of elements become highly dense and narrow in pitch due to the high integration of elements and an increase in the same number of measurements and if there are vertical differences among the electrode pads.

SOLUTION: In this **probe** card, which is a **probing** card to **inspect** the electric characteristics of each of a plurality of IC chips by bringing corresponding **probes** into contact with the plurality of IC chips each formed in a wafer, a **probe** 3 is comprised of a membrane-shaped base end part 3A formed with a constant membrane thickness along the whole circumference of the surface of a base end part of a vertical cone, a membrane-shaped contact terminal part 38 formed along the surface of an apex part of the vertical cone, and a membrane-shaped connecting part 3C spirally wound up from the base end part 3A to connect the contact terminal part 3B to the base end part 3A.

21/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06655634
PROBING CARD

PUB. NO.: 2000-241457 [JP 2000241457 A]
PUBLISHED: September 08, 2000 (20000908)
INVENTOR(s): **TAKEKOSHI KIYOSHI**
APPLICANT(s): TOKYO ELECTRON LTD
APPL. NO.: 11-049171 [JP 9949171]
FILED: February 25, 1999 (19990225)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **probing** card capable of increasing the number of arrangement by highly integrating **probes** in response to arrangement of electrodes, even if the number of electrodes of an element is increased to be highly densified by high integration of the elements, increase of the number of measurement thereof or the like, and capable of executing highly reliable inspection by bringing surely all **probes** into contact with the electrodes of the element.

SOLUTION: This **probing** card 1 executes an electric characteristic **inspection** of each **IC chip** by bringing a **probe** 3 into contact with each of plural IC chips formed on a wafer. The **probe** 3 has a prism-shaped projection 31 formed on a substrate 2, a spacer 32 fixed on the upper end face of the prism-shaped projection 31, a springy spiral plate 33 having one end fixed on the spacer 32, and a contact terminal 34 fixed on the other end of the spiral plate 33. The part having the contact terminal 34 of the spiral plate 33 is formed as a free end.

21/3,AB/11 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06470361
CONTACTOR

PUB. NO.: 2000-055936 [JP 2000055936 A]
PUBLISHED: February 25, 2000 (20000225)
INVENTOR(s): HAGIWARA JUNICHI
IINO SHINJI
APPLICANT(s): TOKYO ELECTRON LTD
APPL. NO.: 10-241036 [JP 98241036]
FILED: August 12, 1998 (19980812)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a contactor which has a high degree of freedom in the arrangement of its **probe** terminals, is capable of arranging the **probe** terminals according to any electrode arrangement of a body to be inspected and further simultaneously inspecting a plurality of elements formed in a body to be inspected, is seldom thermally affected

at the time of inspection, is superior in contacting/property, performs accurate and reliable contact, and is capable of performing highly accurate inspection.
SOLUTION: This contactor 1 is simultaneously brought into contact with 16 or 32 pieces of **chips** and performs electric **inspection** on a wafer a few times. The contactor 1 is provided with a plurality of first electrodes 3 arranged on the surface of a silicon substrate 2 and **probe** terminals 4 each provided for the electrodes 3. The **probe** terminal 4 comprises a conductive supporting column 7 erected on the first electrode 3, a cantilever spring 8 conduction-freely cantilevered and supported at the upper end of the conductive supporting column 7, a bump 9 supported at the free end part of the cantilever spring 8.

21/3,AB/12 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04226450
PROBE CARD

PUB. NO.: 05-218150 [JP 5218150 A]
PUBLISHED: August 27, 1993 (19930827)
INVENTOR(s): **IINO SHINJI**
KUBOTA TAMIO
YOKOTA KEIICHI
APPLICANT(s): TOKYO ELECTRON YAMANASHI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-308928 [JP 92308928]
FILED: November 18, 1992 (19921118)
JOURNAL: Section: E, Section No. 1470, Vol. 17, No. 657, Pg. 79, December 06, 1993 (19931206)

ABSTRACT

PURPOSE: To provide a **probe** card used for a **probing** test machine for **inspecting** the electric characteristics of a semiconductor chip circuit or LCD board circuit.

CONSTITUTION: The title **probe** card is one used for a **probing** test machine which transmits or receives test signals from a circuit through the pads of a semiconductor **chip** and **inspects** the electric characteristics of the circuit. The **probe** card has a support plate 31, a flexible printed circuit board containing a flexible film base material supported by this support plate and having a circuit printed on this film base material and connected to a tester electrically, contactors 42 connected electrically to the printed circuit and brought into contact with the pads one to one, and cushion materials 33 provided to back up sections where the contactors are fitted. When the contactors are brought into contact with the pads, the cushion materials deform elastically, and the contact between the contactors and the pads becomes better.

21/3,AB/13 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03496246
PROBING CARD

PUB. NO.: 03-159146 [JP 3159146 A]
PUBLISHED: July 09, 1991 (19910709)
INVENTOR(s): KOIKE HISASHI
TAKEKOSHI KIYOSHI
IKEDA TORU
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-297989 [JP 89297989]
FILED: November 16, 1989 (19891116)
JOURNAL: Section: E, Section No. 1119, Vol. 15, No. 394, Pg. 56, October 07, 1991 (19911007)

ABSTRACT

PURPOSE: To ensure registration of **probes** to allow the **probe** which enables fine pinching to come into precision contact with all the **electrode pads** of an **inspection** object by constituting a **probing** card by bonding a **probe** needle plate formed by printing-technique to a tapered base provided to a card main body.

CONSTITUTION: A proving card is constituted by bonding a **probe** needle plate 2 formed by printing technique to a tapered base 3 provided to a card main body 1. For example, a proving card is constituted by positioning and fixing a quartz **probe** 2 as a **probe** needle plate to a printed board 1 as a card main body. The quartz **probe** 2 forms an electrode pattern by etching technique after sputtering a metallic layer on a quartz plate and sputtering gold thereon. The electrode pattern of the quartz **probe** 2 is composed of a comb-like electrode needle part 2a, a wiring part 2b and a pad part 2c for contact with a pad. The quartz **probe** 2 is bonded to a tapered side 3a of the tapered base 3 formed by glass or ceramics, etc., by aclylic resin adhesive, etc.

23/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03270676 INSPEC Abstract Number: B89001534
Title: Optical **inspection** system for PCB **chip** mounting
Author(s): Arakawa, T.; Suzuki, N.; Matsumoto, Y.; Nakagawa, T.; Kawahara, T.; **Kataoka, K.**; Ishibashi, T.
Author Affiliation: Inf. Syst. Center, Sanyo Electric Co. Ltd., Osaka, Japan
Journal: Sanyo Technical Review vol.20, no.2 p.104-10
Publication Date: 1988 Country of Publication: Japan
CODEN: STRVD8 ISSN: 0285-516X
Language: Japanese
Abstract: Describes a system that is used to check the mounted condition of chip components, such as missing chips or chips inserted in wrong locations, on a PCB. Chips come in many different shapes, sizes and colors, and PCBs also have many different colors and circuit patterns. To efficiently deal with the complex image presented by chips mounted on a PCB, a gray scale image processing technique has been developed. The initial operation involves dividing the PCB into small areas (cells) and to record each cell's image with a CCD camera. The next step detects error by processing this image through the use of parallel pipeline processors. The average time for checking a chip is 0.08 sec. and the inspection accuracy is 99.99%.
Subfile: B

23/3,AB/2 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10318892 Genuine Article#: 511KY Number of References: 21
Title: Poly(vinyl chloride) membrane electrode for a stimulant, phentermine, using tris(2-ethylhexyl) phosphate as a solvent mediator (ABSTRACT AVAILABLE)
Author(s): Katsu T (REPRINT) ; Ido K; **Kataoka K**
Corporate Source: Okayama Univ,Fac Pharmaceut Sci,Tsushima/Okayama 7008530/Japan/ (REPRINT); Okayama Univ,Fac Pharmaceut Sci,Tsushima/Okayama 7008530/Japan/; Minist Finance,Cent Customs Lab,Kashiwa/Chiba 2770882/Japan/
Journal: SENSORS AND ACTUATORS B-CHEMICAL, 2002, V81, N2-3 (JAN 5), P 267-272
ISSN: 0925-4005 Publication date: 20020105
Publisher: ELSEVIER SCIENCE SA, PO BOX 564, 1001 LAUSANNE, SWITZERLAND
Language: English Document Type: ARTICLE
Abstract: Tris(2-ethylhexyl) phosphate was an effective solvent mediator for constructing a poly(vinyl chloride) (PVC) membrane electrode responsive to a stimulant, phentermine, in combination with an ion-exchanger, sodium tetrakis[3,5-bis(2-methoxyhexafluoro-2-propyl)phenyl]borate (NaHFPB). This electrode discriminated between phentermine and analogous compounds and showed remarkably little interference by lipophilic quaternary ammonium ions, as well as inorganic cations, to almost the same degree of an electrode using the recently developed phentermine ionophore, N,N-dioctadecyl-N',N'-dipropyl-3,6-dioxaoctanediamide. The present electrode exhibited a near-Nernstian response to phentermine in

the concentration range of 2 x 10(-6) to 1 x 10(-2) M with a slope of 58.8 mV per concentration decade in 0.1 M MgCl2. The limit of detection was 1 X 10(-6) M. This electrode was applied to determine phentermine in ion-exchange resin complexes containing this stimulant. (C) 2002 Elsevier Science B.V. All rights reserved.

23/3,AB/3 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03774834 JICST ACCESSION NUMBER: 98A0822128 FILE SEGMENT: JICST-E
IC Quality Assurance.
KATAOKA KOZO (1)
(1) Fuji Electr. Co., Ltd.
Fuji Jiho(Fuji Electric Journal), 1998, VOL.71,NO.8, PAGE.465-467, FIG.6, TBL.1
JOURNAL NUMBER: F0080AAJ ISSN NO: 0367-3332 CODEN: FUJIA
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes basic thought about IC(integrated circuit) quality assurance at the four stages of new product development, preparation for production, production, and delivery. At each stage, analysis data is fed back to the source to maintain or improve the product quality and reliability. Lists of analysis methods and analysis examples, and failure modes and causes derived from the valuable **IC** failure **analysis** data are quoted. (author abst.)

23/3,AB/4 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03010329 JICST ACCESSION NUMBER: 96A0842896 FILE SEGMENT: JICST-E
Quality Assurance of Integrated Circuits.
KATAOKA KOZO (1); KOYAMA YUKIO (1)
(1) Fuji Electr. Co., Ltd., Matsumoto Factory
Fuji Jiho(Fuji Electric Journal), 1996, VOL.69,NO.8, PAGE.448-449, FIG.5, TBL.1
JOURNAL NUMBER: F0080AAJ ISSN NO: 0367-3332 CODEN: FUJIA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.08
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes the basic concept of quality assurance of integrated circuits (IC's) in four stages of new product planning, development, design, to shipping, and gives the details on the important matters among them. One is **IC** fault **analyses** and fault mechanisms, in which IC fault modes, a list of fault causes, and their typical photos are shown. The other is feedback of analysis data to the source to maintain and improve the reliability of quality, for which an explanation is given. (author abst.)

23/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05973223
VACUUM CONTACTOR

PUB. NO.: 10-256323 [JP 10256323 A]
PUBLISHED: September 25, 1998 (19980925)
INVENTOR(s): **IINO SHINJI**
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-100881 [JP 97100881]
FILED: March 07, 1997 (19970307)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a vacuum contactor, which can accurately perform electrical inspection of each semiconductor element by accurately contacting the **inspecting electrode** of a semiconductor wafer with a contact terminal without loading an unbalanced load on a mounting stage.

SOLUTION: This vacuum contactor 1 has a contactor main body 2, which has a plurality of protruding terminals 2A that can be in contact with at least one-chip electrode pad of a wafer W, and a chamber 3 forming a space including the protruding part, wherein the contact main body 2 penetrates so as to form a unitary body. At the lower surface of the surrounding wall of the chamber 3, an O ring 6, which is in contact with the wafer W and keeps the airtightness of an inner space, is provided. At the same time, an exhaust pipeline 7 is linked to an exhaust path 3C of the chamber 3. At the time of inspection, the air in the airtight space formed by the chamber 3 and the wafer W is exhausted by the exhausting pipeline 7, and the wafer W is sucked by the vacuum. At the same time, the electrode pad and the corresponding protruding terminal 2A are brought into contact

23/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04019299
INSPECTION METHOD FOR LIQUID CRYSTAL DISPLAY PLATE AND THE SYSTEM

PUB. NO.: 05-010999 [JP 5010999 A]
PUBLISHED: January 19, 1993 (19930119)
INVENTOR(s): **IINO SHINJI**
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-019547 [JP 9119547]
FILED: January 18, 1991 (19910118)
JOURNAL: Section: P, Section No. 1544, Vol. 17, No. 269, Pg. 151, May 25, 1993 (19930525)

ABSTRACT

PURPOSE: To save the process after finding a fault by inspecting an LCD(liquid crystal display) plate before charging the liquid crystal without touching the picture element unit.

CONSTITUTION: **Inspection electrodes** 7 are arranged face to face by way of capacity components on picture element electrodes 3. Each TFT(thin film transistor) 2 for example, on the LCD plate 6 is selected in a matrix method and a pulse is impressed on the gate electrodes of the selected TFT 2. The pulse 10 transmitted to the **inspection electrode** 7 side through the capacity components is detected with a pulse detector 10. By comparing the pulse peak value, for example, with a preset value based on the detected pulse at the judgement part 11, the quality of the picture element is judged.

23/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03132450
CONTROL OF MOVING TABLE FOR SOLDERING **INSPECTOR** FOR **IC** PACKAGE

PUB. NO.: 02-107950 [JP 2107950 A]
PUBLISHED: April 19, 1990 (19900419)
INVENTOR(s): **KATAOKA KENSEI**
WATABE SHUICHI
APPLICANT(s): RHYTHM WATCH CO LTD [360110] (A Japanese Company or Corporation), JP (Japan)
RIZUMU KOKI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-261128 [JP 88261128]
FILED: October 17, 1988 (19881017)
JOURNAL: Section: P, Section No. 1075, Vol. 14, No. 325, Pg. 73, July 12, 1990 (19900712)

ABSTRACT

PURPOSE: To enable stopping of a table at the same position constantly by a method wherein the position of a moving table is stopped at an origin position detecting the position thereof, then moved to the origin position from a fixed direction once shifted off the origin position and stopped detecting the position thereof again.

CONSTITUTION: To determine the origin position of a moving table 40, in regard to an X axis direction, after a mobile plate 41 is moved by a fixed value to the left, the X axis mobile plate 41 is moved to the right at a fixed low speed when a position detection switch SW61 provided on the bottom plate 15 detects a detection piece 48 provided thereon 41, and then the mobile plate 41 is stopped again with the SW61 detecting the position of the mobile plate 41. After the SW61 detects the detection piece 48, a required number of pulses is applied to a driving motor 42 so that the detection piece 48 is inserted accurately into the SW61. In addition, when a position detection SW62 for detecting a right movement limit of the table 40 detects the detection piece 48, the table 40 is moved to the left to detect the detection piece 48 with the SW61. Thereafter, the same operation is performed as mentioned above. The same is done with the operation in a Y-axis direction.

23/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

00285669
INSPECTING SYSTEM FOR **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 53-087669 [JP 53087669 A]
PUBLISHED: August 02, 1978 (19780802)
INVENTOR(s): WADA YASUSHI
INOUE JUNJI
KATAOKA KEISUKE
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 52-002238 [JP 772238]
FILED: January 12, 1977 (19770112)
JOURNAL: Section: E, Section No. 63, Vol. 02, No. 121, Pg. 7114, October 12, 1978 (19781012)

ABSTRACT

PURPOSE: To judge the goodness or not of functions by two-dimensionally analyzing the heat released from an element under operation.

(FILE 'HOME' ENTERED AT 13:46:43 ON 29 SEP 2003)

FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 13:47:48 ON 29 SEP 2003

E JP2001-093303/AP,PRN

L1 6 S E3-E4

E JP2000-249702/AP,PRN

L2 6 S E4

L1 ANSWER 1 OF 6 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2002-328642 [36] WPIX
DNN N2002-257899
TI Semiconductor device inspection method for measuring electrical characteristics, involves applying a voltage between two probes in contact with oxide film to induce fritting and breakage of film.
DC S01 U11
IN IINO, S; ITOH, T; KATAOKA, K; SUGA, T; TAKEKOSHI, K
PA (ITOH-I) ITOH T; (SUGA-I) SUGA T; (TKEL) TOKYO ELECTRON LTD; (ITOK-I) ITO K; (SUGA-I) SUGA Y; (IINO-I) IINO S; (KATA-I) KATAOKA K; (TAKE-I) TAKEKOSHI K
CYC 30
PI US 2002021142 A1 20020221 (200236)* 22p
EP 1182460 A2 20020227 (200236) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2002139542 A 20020517 (200237) 11p
KR 2002015294 A 20020227 (200258)
TW 497194 A 20020801 (200330)
ADT US 2002021142 A1 US 2001-931888 20010820; EP 1182460 A2 EP 2001-119644 20010821; JP 2002139542 A **JP 2001-93303 20010328**; KR 2002015294 A KR 2001-50240 20010821; TW 497194 A TW 2001-120363 20010820
PRAI **JP 2001-93303 20010328**; JP 2000-249702 20000821
AB US2002021142 A UPAB: 20020610
NOVELTY - The method involves bringing two probe electrodes (5A,5B) into contact with oxide film (O) on semiconductor device (D) inspection electrode (P) and applying voltage between them so as to induce fritting and breakage of oxide film. One probe is removed from surface of device using piezo element, bimetal or electrostatic element and the other probe is then used to inspect electrical characteristics of device.
USE - For inspecting electrical characteristics of semiconductor devices on a wafer or packaged semiconductor devices.
ADVANTAGE - Less pressure is required to be applied to the probe to obtain sound electrical contact with the device. Damage done to the device inspection electrode is eliminated and probe life is prolonged. Eliminates the need to clean the probe, thereby improving inspection efficiency.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic of the apparatus used in the method.
Probe electrodes 5A,5B
Semiconductor device D
Oxide film O
Inspection electrode P
Dwg.1/22

L1 ANSWER 2 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 210911606 INPADOC ED 20030729 EW 200330 UP 20030729 UW 200330
TI INSPECTION METHOD AND INSPECTION APPARATUS.
IN IINO, SHINJI; TAKEKOSHI, KIYOSHI; SUGA, TADATOMO; ITOH, TOSHIHIRO; KATAOKA, KENICHI
INS IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITOH TOSHIHIRO; KATAOKA KENICHI
INA JP; JP; JP; JP; JP
PA TOKYO ELECTRON LTD.; SUGA, TADATOMO; ITOH, TOSHIHIRO
PAS TOKYO ELECTRON LTD; SUGA TADATOMO; ITOH TOSHIHIRO

PAA JP; JP; JP
TL English
DT Patent
PIT TWB PATENT
PI TW 497194 B 20020801
AI TW 2001-120363 A 20010820
PRAI JP 2000-249702 A 20000821
JP 2001-93303 A 20010328
AB Disclosed is an inspection method for inspecting the electrical characteristics of a device by bringing an inspecting probe into electrical contact with an inspection electrode. An insulating film formed on the surface of the inspection electrode is broken by utilizing a fritting phenomenon so as to bring the inspection electrode into electrical contact with the inspection electrode.

L1 ANSWER 3 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 177282101 INPADOC ED 20020617 EW 200224 UP 20021002 UW 200239
TI INSPECTION METHOD AND INSPECTION DEVICE.
IN IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITO HISAHIRO; KATAOKA KENICHI
INS IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITO HISAHIRO; KATAOKA KENICHI
PA TOKYO ELECTRON LTD; SUGA TADATOMO; ITO HISAHIRO
PAS TOKYO ELECTRON LTD; SUGA TADATOMO; ITO HISAHIRO
TL English
DT Patent
PIT JPA2 DOCUMENT LAID OPEN TO PUBLIC INSPECTION
PI JP 2002139542 A2 20020517
AI **JP 2001-93303 A 20010328**
PRAI **JP 2001-93303 A 20010328**
JP 2000-249702 A 20000821

L1 ANSWER 4 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 169691783 INPADOC ED 20020319 EW 200211 UP 20020319 UW 200211
TI INSPECTION METHOD AND INSPECTION APPARATUS.
IN IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITOH TOSHIHIRO; KATAOKA KENICHI
INS IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITOH TOSHIHIRO; KATAOKA KENICHI
INA JP; JP; JP; JP; JP
PA IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITOH TOSHIHIRO; KATAOKA KENICHI
PAS IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITOH TOSHIHIRO; KATAOKA KENICHI
PAA JP; JP; JP; JP; JP
DT Patent
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI US 2002021142 AA 20020221
AI US 2001-931888 A 20010820
PRAI JP 2000-249702 A 20000821
JP 2001-93303 A 20010328
AB Disclosed is an inspection method for inspecting the electrical characteristics of a device by bringing an inspecting probe into electrical contact with an inspection electrode. An insulating film

formed on the surface of the inspection electrode is broken by utilizing a fritting phenomenon so as to bring the inspection electrode into electrical contact with the inspection electrode.

L1 ANSWER 5 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 2
AN 169198083 INPADOC ED 20030825 EW 200334 UP 20030825 UW 200334
TI FRITTING INSPECTION METHOD AND APPARATUS.
IN IINO, SHINJI; TAKEKOSHI, KIYOSHI; SUGA, TADATOMO; ITOH, TOSHIHIRO; KATAOKA, KENICHI
INS IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITOH TOSHIHIRO; KATAOKA KENICHI
INA JP; JP; JP; JP; JP
PA TOKYO ELECTRON LIMITED; SUGA, TADATOMO; ITOH, TOSHIHIRO
PAS TOKYO ELECTRON LTD; SUGA TADATOMO; ITOH TOSHIHIRO
PAA JP; JP; JP
TL English; French; German
LA English
DT Patent
PIT EPA3 PUBL. OF SEARCH REPORT
PI EP 1182460 A3 20030820
DS R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
AI EP 2001-119644 A 20010821
PRAI JP 2000-249702 A 20000821
JP 2001-93303 A 20010328

L1 ANSWER 6 OF 6 JAPIO (C) 2003 JPO on STN
AN 2002-139542 JAPIO
TI INSPECTION METHOD AND INSPECTION DEVICE
IN IINO SHINJI; TAKEKOSHI KIYOSHI; SUGA TADATOMO; ITO HISAHIRO; KATAOKA KENICHI
PA TOKYO ELECTRON LTD
SUGA TADATOMO
ITO HISAHIRO
PI JP 2002139542 A 20020517 Heisei
AI **JP 2001-93303** (JP2001093303 Heisei) 20010328
PRAI JP 2000-249702 20000821
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To solve such problems in an inspection method that the service life of a probe N is shortened by scrubbing and that yield of a device is reduced by damaging the inspection electrode P as shown in (b) of figure 7 when the probe N is brought into contact with an inspection electrode P electrically by scrubbing operation.
SOLUTION: This inspection method for executing electric characteristic inspection of the device by bringing an inspection probe 12A into electric contact with the inspection electrode P, has a contact process for bringing the inspection probe 12A into electric contact with the inspection electrode P by breaking an insulating coat O of the inspection electrode P by utilizing fritting phenomenon.
COPYRIGHT: (C)2002,JPO